VALERIU BEIU PUBLICATIONS

OVERVIEW	PUBLISHED		ACCEPTED	
BOOKS	2		3	
CHAPTERS	8	(7 INVITED)	5	
PATENTS	20			
JOURNALS	43	(2 INVITED)	3	(1 INVITED)
CONFERENCES	225	(28 INVITED)		
TOTAL	**309**	**(38 INVITED, 8 BEST PAPER AWARDS)**		
OTHER CONFERENCES	53	(*7 INVITED, 1 BEST PAPER AWARD*)		
TECHNICAL REPORTS	73			

BOOKS 2

– V. Beiu and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures
Book in progress (contract signed with World Scientific)

– V. Beiu: VLSI Complexity of Discrete Neural Networks
Book in progress (contract signed with Taylor & Francis)

– V. Beiu, R. Andonie, and R. Dogaru: Fundamental Problems of Neural Networks
Book in progress (contract signed with Technical Printing House)

B_2 V. Beiu and S. Harous (Eds.): Innovations
IEEE Press, November 2014 (ISBN 9781479972128) 1–132
https://doi.org/10.1109/INNOVATIONS.2014.6985768

B_1 A. Schmid, S. Goel, W. Wang, V. Beiu, and S. Carrara (Eds.): Nano-Net
Springer, LNICS, October 2009 (ISBN 9783642024276) 1–286
https://doi.org/10.1007/978-3-642-04850-0

··· V. Beiu: Neural Networks Using Threshold Gates
A Complexity Analysis of Their Area- and Time-Efficient VLSI Implementations
PhD dissertation (*summa cum laude*), Katholieke Universiteit Leuven, Leuven, Belgium
U.D.C. 621.3.04977: 681.3*C13 (x-27-151779-3), May 1994 1–222

CHAPTERS (7 INVITED) 8

– V. Beiu and W. Ibrahim: On Enabling Redundant Designs for Nano Computations
In V. Beiu and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures

– V. Beiu, J.M. Quintana, and M.J. Avedillo
Threshold Logic Design and Implementations: From the Early Days into the Nanoera
In V. Beiu and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures

– M.H. Sulieman and V. Beiu
From Single Electron Technology (SET) Full Adders to Optimal Practical SET Adders
In V. Beiu and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures

– V. Beiu and U. Rückert: Roadmap for Nano Architectures
In V. Beiu and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures

– J. Nyathi, and V. Beiu: Advanced Techniques for Reducing Power Consumption
In V. Beiu and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures

Ch_8 V. Beiu, L. Zhang, A. Beg, W. Ibrahim, and M. Tache: Axon-Inspired Communication Systems ***Invited$_7$***
Chapter 15 in J.E. Morris and K. Iniewski (Eds.): Nanoelectronic Device Applications
Handbook, CRC/Taylor & Francis (UK/USA), 2013 (ISBN 9781466565234) 193–208

Ch$_7$ A. Beg, M.H. Sulieman, V. Beiu, and W. Ibrahim: Low-Power Reliable Nano Adders ***Invited$_6$***
Chapter 6 in J.E. Morris and K. Iniewski (Eds.): Nanoelectronic Device Applications
Handbook, CRC/Taylor & Francis (UK/USA), 2013 (ISBN 9781466565234) 67–75

Ch$_6$ V. Beiu, W. Ibrahim, and S. Lazarova-Molnar
On Device-level Majority von Neumann Multiplexing ***Invited$_5$***
Chapter 72 in J.R. Rabuñal et al. (Eds.): Encyclopedia of Artificial Intelligence
IGI Global, USA (Hershey, PA) and UK (London), 2009 (ISBN 9781599048499) 471–479
https://doi.org/10.4018/978-1-59904-849-9.ch072

Ch$_5$ V. Beiu and W. Ibrahim: On Computing Nano-Architectures Using Unreliable Nano-Devices ***Invited$_4$***
Chapter 12 in S.E. Lyshevski (Ed.): Nano- and Molecular-Electronics Handbook
Taylor & Francis (UK/USA), May 2007 (ISBN 9780849385285) 1–49

Ch$_4$ V. Beiu: Entropy, Constructive Neural Learning, and VLSI Efficiency ***Invited$_3$***
In R. Andonie, and D. Grosu (Eds.): Neural Priorities in Data Transmission and EDA
Tempus SJEP 8180-94, “Transilvania” Univ. of Braşov, Braşov, Romania, 1998 38–74

Ch$_3$ V. Beiu: Constant Fan-in Discrete Neural Networks Are VLSI-Optimal
Chapter 12 in S.W. Ellacott, J.C. Mason, and I.J. Anderson (Eds.)
Mathematics of Neural Networks Models, Algorithms and Applications
Kluwer Academic, Boston, MA, USA, 1997 (ISBN 9781461377948) 89–94
https://doi.org/10.1007/978-1-4615-6099-9_12

Ch$_2$ V. Beiu: Digital Integrated Circuit Implementations (of Neural Networks) ***Invited$_2$***
Chapter E1.4 in E. Fiesler, and R. Beale (Eds.): Handbook of Neural Computations
Institute of Physics, New York, NY, USA, 1996 (ISBN 9780750303125) E1.4.1–34

Ch$_1$ V. Beiu: Optimal VLSI Implementations of Neural Networks ***Invited$_1$***
Chapter 18 in J.G. Taylor (Ed.): Neural Networks and Their Applications
John Wiley & Sons, Chichester, UK, 1996 (ISBN 9780471962823) 255–276

PATENTS (SINGLE AUTHOR ON ALL OF THEM) ***20***

– V. Beiu: Procedure Enabling Statistical Meaningful Evaluation of Any Physical Feature
or Figure-of-Merit of a Digital or Analog Circuit
UAEU Intellectual Property Disclosure, Jul. 16, 2014 & Feb. 11, 2015 (Rouse Ref. U0018-00167)

P$_{20}$ V. Beiu: Low-Power Differential Conductance-Based Logic Gate and Method of Operation Thereof
(Washington, DC, USA, June 17, 2003) 1–18
US40319573 https://patentscope.wipo.int/search/en/detail.jsf?docId=US40319573

P$_{18, 19}$ V. Beiu: Microprocessor and a Digital Signal Processor Including Adder and Multiplier Circuits
Employing Logic Gates Having Discrete and Weighted Inputs (February 4, 2003) 1–14
US39973941 https://patentscope.wipo.int/search/en/detail.jsf?docId=US39973941
US39287083 https://patentscope.wipo.int/search/en/detail.jsf?docId=US39287083

P$_{17}$ V. Beiu: Adder Circuits Employing Logic Gates Having Discrete Weighted Inputs and a
Method of Operation Therewith (Washington, DC, USA, December 31, 2002) 1–13
US39287082 https://patentscope.wipo.int/search/en/detail.jsf?docId=US39287082

P$_{13\text{-}16}$ V. Beiu: Adder Having Reduced Number of Internal Layers and Method of Operation Thereof
(Washington, DC, USA, August 20, 2002) 1–11
AU180986431 https://patentscope.wipo.int/search/en/detail.jsf?docId=AU180986431
TW 493139 https://twpat1.tipo.gov.tw/tipotwoc/tipotwekm?!!FR_493139
US39682800 https://patentscope.wipo.int/search/en/detail.jsf?docId=US39682800
WO2001023992 https://patentscope.wipo.int/search/en/detail.jsf?docId=WO2001023992

$P_{9\text{-}12}$ V. Beiu: Noise Tolerant Conductance-Based Logic Gate and Methods of Operation and
Manufacturing Thereof (Washington, DC, USA, August 6, 2002) 1–16
AU180951667 https://patentscope.wipo.int/search/en/detail.jsf?docId=AU180951667
TW 483249 https://twpat1.tipo.gov.tw/tipotwoc/tipotwekm?!!FR_483249
US39680498 https://patentscope.wipo.int/search/en/detail.jsf?docId=US39680498
WO2001024367 https://patentscope.wipo.int/search/en/detail.jsf?docId=WO2001024367

P_{8} V. Beiu: Logic Gate Having Reduced Power Dissipation and Method of Operation Thereof
(Washington, DC, USA, July 10, 2001) 1–19
US39453725 https://patentscope.wipo.int/search/en/detail.jsf?docId=US39453725

$P_{2\text{-}7}$ V. Beiu: Adder and Multiplier Circuits Employing Logic Gates Having Discrete, Weighted Inputs
and Methods of Performing Combinatorial Operations Therewith (March 20, 2001) 1–14
AU180873674 https://patentscope.wipo.int/search/en/detail.jsf?docId=AU180873674
TW 481774 https://twpat1.tipo.gov.tw/tipotwoc/tipotwekm?!!FR_481774
US40229075 https://patentscope.wipo.int/search/en/detail.jsf?docId=US40229075
US39353335 https://patentscope.wipo.int/search/en/detail.jsf?docId=US39353335
US39287081 https://patentscope.wipo.int/search/en/detail.jsf?docId=US39287081
WO2000017802 https://patentscope.wipo.int/search/en/detail.jsf?docId=WO2000017802

P_{1} V. Beiu: LSI Unit for Mutual Exclusion
Dispozitiv de excludere mutuala a unor sarcini referitoare la controlul asupra unor resurse 1–12
RO 84763, April 26, 1984 https://patents.google.com/patent/RO84763B1/en

JOURNALS (3 INVITED) 43

··· V. Beiu et al.: The Curse of Constant Failure Rates, Inputs and Averaging – A Comprehensive Review In planning
··· V. Beiu et al.: Brain-inspired Computing Revisited – Why Energy Consumption Is So Elusive In progress
··· V. Beiu et al.: Revisiting Schmitt Trigger Tolerance to Variations In progress
··· V. Beiu, R.-M. Beiu, and V. Dragoi: The Trustworthy Wings of the Mysterious Butterflies To be submitted

J_{46} S.R. Cowell, S. Hoara, and V. Beiu: Approximating Hammocks' Reliability with Beta Distributions
Intl. J. Comp. Comm. & Ctrl. (IF ~ 2.635, SJR ~ 0.499) Accepted

J_{45} V. Beiu: Brain Inspired Nano Architectures ***Invited***$_3$
Intl. J. Comp. Comm. & Ctrl. (IF ~ 2.635, SJR ~ 0.499) Accepted

J_{44} M. Tache and V. Beiu: When Non-Gaussian Distributions Have to Be Considered
Theory and Applications of Mathematics & Computer Science Accepted

J_{43} V. Dragoi and V. Beiu
Which Coefficients Matter Most – Consecutive-k-out-of-n:F Systems Revisited
IEEE Trans. Reliab., vol. 73, no. 3, Sep. 2024 (IF ~ 5.9, SJR ~ 1.296) 1633–1646
https://doi.org/10.1109/TR.2024.3353908

J_{42} M. Nagy, S.R. Cowell, and V. Beiu
On the Construction of 3D Fibonacci Spirals
Mathematics, vol. 12, no. 2, Jan. 2024 (IF ~ 2.4, SJR ~ 0.446) art. 201 (1–19)
https://doi.org/10.3390/math12020201

J_{41} M. Jianu, L. Daus, V. Dragoi, and V. Beiu
The Roots of the Reliability Polynomials of Circular Consecutive-k-out-of-n:F Systems
Mathematics, vol. 11, no. 20, Oct. 2023 (IF ~ 2.4, SJR ~ 0.446) art. 4252 (1–12)
https://doi.org/10.3390/math11204252

J_{40} M. Jianu, L. Daus, V. Dragoi, and V. Beiu
Reliability Polynomials of Consecutive-k-out-of-n:F Systems Have Unbounded Roots
Networks, vol. 82, no. 3, Oct. 2023 (IF $\sim$ 2.1, SJR $\sim$ 0.908) 222–228
https://doi.org/10.1002/net.22168

J_{39} V. Dragoi and V. Beiu
Fast Reliability Ranking of Matchstick Minimal Networks ***Highly cited***
Networks, vol. 79, no. 4, Jun. 2022 (IF = 2.1, SJR = 0.908) 479–500
https://doi.org/10.1002/net.22064

J_{38} M. Nagy, S.R. Cowell, and V. Beiu
Survey of Cubic Fibonacci Identities – When Cuboids Carry Weight
Intl. J. Comp. Comm. & Ctrl., vol. 17, no. 2, Apr. 2022 (IF = 2.7, SJR $\sim$ 0.458) art. 4616 (1–20)
https://doi.org/10.15837/ijccc.2022.2.4616

J_{37} V. Beiu, L. Daus, M. Jianu, A. Mihai, and I. Mihai
On a Surface Associated with Pascal's Triangle
Symmetry, vol. 14, no. 2, Feb. 2022 (IF = 2.7, SJR = 0.483) art. 411 (1–12)
https://doi.org/10.3390/sym14020411

J_{36} V. Dragoi, S.R. Cowell, and V. Beiu
Four Input Sorter Good, Larger Ones Not So Good
IEEE Trans. Nanotech., vol. 20, Sep. 2021 (IF = 2.967, SJR = 0.577) 775–783
https://doi.org/10.1109/TNANO.2021.3113731

J_{35} V. Dragoi and V. Beiu
Studying the Binary Erasure Polarization Subchannels Using Network Reliability
IEEE Comm. Lett., vol. 24, no. 1, Jan. 2020 (IF = 3.436, SJR = 0.929) 62–66
https://doi.org/10.1109/LCOMM.2019.2947910

J_{34} V. Dragoi, S.R. Cowell, V. Beiu, S. Hoara, and P. Gaspar
How Reliable Are Compositions of Series and Parallel Networks
Compared with Hammocks?
Intl. J. Comp. Comm. & Ctrl., vol. 13, no. 5, Oct. 2018 (IF = 1.585, SJR = 0.368) 772–791
https://doi.org/10.15837/ijccc.2018.5.3354

J_{33} M. Tache, W. Ibrahim, F. Kharbash, and V. Beiu
Reliability and Performance of Optimised Schmitt Trigger Gates
IET Journal of Engineering, vol. 2018, no. 8, Aug. 2018 735–744
https://doi.org/10.1049/joe.2018.0091

J_{32} S.R. Cowell, M. Nagy, and V. Beiu
A Proof of a Generic Fibonacci Identity from Wolfram's MathWorld
Theory and Applications of Mathematics & Computer Science, vol. 8, no. 1, Apr. 2018 60–63
http://www.uav.ro/applications/se/journal/index.php/TAMCS/article/view/175
https://typeset.io/pdf/a-proof-of-a-generic-fibonacci-identity-from-wolfram-s-53do8mmhhy.pdf

J_{31} S.R. Cowell, V. Beiu, L. Daus, and P. Poulin
On the Exact Reliability Enhancements of Small Hammock Networks
IEEE Access, vol. 6, no. 1, Apr. 2018 (IF = 4.098, SJR = 0.609) 25411–25426
https://doi.org/10.1109/ACCESS.2018.2828036

J_{30} R.-M. Beiu, V. Beiu, and V.-F. Duma
Fiber Optic Mechanical Deformation Sensors Employing Perpendicular Photonic Crystals
Optics Express, vol. 25, no. 19, 18 Sep. 2017 (IF = 3.561, SJR = 1.473) 23388–23398
https://doi.org/10.1364/OE.25.023388

J_{29} V. Beiu and M. Tache
On Threshold Voltage Variation-Tolerant Designs
Theory and Applications of Mathematics & Computer Science, vol. 7, no. 1, Apr. 2017 47–58
http://www.uav.ro/stiinte_exacte/journal/index.php/TAMCS/article/view/159
https://typeset.io/journals/theory-and-applications-of-mathematics-computer-science-ac6w1jen/2017

J_{28} V. Beiu and L. Daus
Reliability Bounds for Two Dimensional Consecutive Systems ***Invited$_2$***
Nano Communication Networks, vol. 6, no. 3, Sep. 2015 (SJR = 0.469)
Special Issue on Biological Information and Communication Technology 145–152
https://doi.org/10.1016/j.nancom.2015.04.003

J_{27} L. Daus and V. Beiu
Lower and Upper Reliability Bounds for Consecutive-*k*-out-of-*n*:*F* Systems
IEEE Transactions on Reliability, vol. 64, no. 3, Sep. 2015 (IF = 2.287, SJR = 1.930) 1128–1135
https://doi.org/10.1109/TR.2015.2417527

J_{26} M. Tache, V. Beiu, W. Ibrahim, F. Kharbash, and M. Alioto
Enhancing the Static Noise Margins by Sizing Length for ***Invited$_1$***
Ultra-Low Voltage/Power/Energy Gates
Journal of Low Power Electronics, vol. 10, no. 1, Mar. 2014 (SJR = 0.186) 137–148
https://doi.org/10.1166/jolpe.2014.1305

J_{25} G. Wendin, D. Vuillaume, M. Calame, S. Yitzchaik, C. Gamrat, G. Cuniberti, and V. Beiu
SYMONE Project: SYnaptic MOlecular NEtworks for Bio-inspired Information Processing
Journal of Unconventional Computing, vol. 8, no. 4, Nov. 2012 (IF = 0.431, SJR = 0.205) 325–332
http://www.oldcitypublishing.com/journals/ijuc-home/ijuc-issue-contents/ijuc-volume-8-number-4-2012/ijuc-8-4-p-325-332/

J_{24} W. Ibrahim, V. Beiu, and A. Beg
Optimum Reliability Sizing for Complementary Metal Oxide Semiconductor Gates
IEEE Transactions on Reliability, vol. 61, no. 3, Sep. 2012 (IF = 2.293, SJR = 1.516) 675–686
https://doi.org/10.1109/TR.2012.2206249

J_{23} W. Ibrahim, V. Beiu, and A. Beg
GREDA: A Fast and More Accurate CMOS Gates Reliability EDA Tool
IEEE Transactions on Computer-Aided Design of Integrated Circuits & Systems
vol. 31, no. 4, Apr. 2012 (IF = 1.093, SJR = 0.790) 509–521
https://doi.org/10.1109/TCAD.2011.2176123

J_{22} W. Ibrahim and V. Beiu
Using Bayesian Networks to Accurately Calculate the Reliability of CMOS Gates
IEEE Transactions on Reliability, vol. 60, no. 3, Sep. 2011 (IF = 1.285, SJR = 1.337) 538–549
https://doi.org/10.1109/TR.2011.2161032

J_{21} V. Beiu and W. Ibrahim
Devices and Input Vectors Are Shaping von Neumann Multiplexing
IEEE Transactions on Nanotechnology, vol. 10, no. 3, May 2011 (IF = 2.292, SJR = 1.271) 606–616
https://doi.org/10.1109/TNANO.2010.2059036

J_{20} V. Beiu, B.A.M. Madappuram, P.M. Kelly, and L.J. McDaid
On Two-layer Brain-inspired Hierarchical Topologies — A Rent's Rule Approach
Transactions on High-Performance Embedded Architecture and Compilers (HiPEAC) IV
P. Stenström (Ed.), Springer LNCS 6769, Jan. 2011 311–333
https://doi.org/10.1007/978-3-642-24568-8_16

J_{19} W. Ibrahim and V. Beiu
Threshold Voltage Variations Make Full Adders Reliabilities Similar
IEEE Transactions on Nanotechnology, vol. 9, no. 6, Nov. 2010 (IF = 1.864, SJR = 1.203) 664–667
https://doi.org/10.1109/TNANO.2010.2066573

J_{18} W. Ibrahim, V. Beiu, and M.H. Sulieman
On the Reliability of Majority Gates Full Adders
IEEE Transactions on Nanotechnology, vol. 7, no. 1, Jan. 2008 (IF = 2.154, SJR = 1.387) 56–67
https://doi.org/10.1109/TNANO.2007.915203

J_{17} V. Beiu, S. Aunet, J. Nyathi, R.R. Rydberg III, and W. Ibrahim
Serial Addition: Locally Connected Architectures
IEEE Transactions on Circuits & Systems I, vol. 54, no. 11, Nov. 2007 (IF = 1.204, SJR = 1.438)
Special Issue on Circuits and Computing Architectures for Nanotechnology 2564–2579
https://doi.org/10.1109/TCSI.2007.907885

J_{16} M.H. Sulieman, and V. Beiu
On Single Electron Technology Full Adders
IEEE Transactions on Nanotechnology, vol. 4, no. 6, Nov. 2005 (IF = 2.112, SJR = 2.455) 669–680
https://doi.org/10.1109/TNANO.2005.858609

J_{15} S. Roy and V. Beiu
Majority Multiplexing — Economical Redundant Fault-Tolerant Design for Nano Architectures
IEEE Transactions on Nanotechnology, vol. 4, no. 4, Jul. 2005 (IF = 2.112, SJR = 2.455) 441–451
https://doi.org/10.1109/TNANO.2005.851251

J_{14} V. Beiu, J.M. Quintana, and M.J. Avedillo
VLSI Implementations of Threshold Gates — A Comprehensive Survey
IEEE Transactions on Neural Networks, vol. 14, no. 5, May 2003 (IF = 1.666, SJR = 1.727)
Special Issue on Hardware Implementations of Neural Networks 1217–1243
https://doi.org/10.1109/TNN.2003.816365

J_{13} V. Beiu: On VLSI-Optimal Neural Computations
Journal of Control Engineering & Applied Informatics, vol. 4, no. 2, Feb. 2002 (IF later) 5–20
http://www.ceai.srait.ro/index.php?journal=ceai&page=article&op=view&path%5B%5D=89

J_{12} V. Beiu: On Optimal Computations Using Perceptrons
Journal of Control Engineering & Applied Informatics, vol. 4, no. 1, Jan. 2002 (IF later) 33–43
http://www.ceai.srait.ro/index.php?journal=ceai&page=article&op=view&path%5B%5D=84

J_{11} V. Beiu, S. Draghici, and T. De Pauw
A Constructive Approach to Calculating Lower Entropy Bounds
Neural Processing Letters, vol. 9, no. 1, Feb. 1999 (IF = 0.405, SJR = 1.162) 1–12
https://doi.org/10.1023/A:1018659009494

J_{10} V. Beiu and H.E. Makaruk
Deeper Sparsely Nets Can Be Optimal
Neural Processing Letters, vol. 8, no. 3, Dec. 1998 (IF = 0.286, SJR later) 201–210
https://doi.org/10.1023/A:1009665432594

J_{9} V. Beiu: On the Circuit and VLSI Complexity of Threshold Gate COMPARISON
Neurocomputing, vol. 19, no. 1, Apr. 1998 (IF = 0.453, SJR later) 77–98
https://doi.org/10.1016/S0925-2312(97)00099-4

J_{8} V. Beiu: Reduced Complexity Constructive Learning Algorithm
Neural Network World, vol. 8, no. 1-3, Jan. 1998 (IF later, SJR later) 1–38

J$_7$ V. Beiu and J.G. Taylor
On the Circuit Complexity of Sigmoid Feedforward Neural Networks
Neural Networks, vol. 9, no. 7, Oct. 1996 (IF = 1.325, SJR later) 1155–1171
https://doi.org/10.1016/0893-6080(96)00130-X

J$_6$ V. Beiu: Entropy Bounds for Classification Algorithms
Neural Network World, vol. 6, no. 4, Jul. 1996 (IF later, SJR later) 497–505

J$_5$ V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins: Close Approximations of Sigmoid Functions by Sum of Steps for VLSI Implementation of Neural Networks
Scientific Annals of “Al. I. Cuza” University of Iaşi, vol. 40, no. 3, 1994 (IF later) 5–34
https://www.info.uaic.ro/en/sacs_articles/close-approximations-of-sigmoid-functions-by-sum-of-step-for-vlsi-implementation-of-neural-networks/

J$_4$ V. Beiu, D.C. Ioan, and M.C. Dumbrava
Continuous Boltzmann Machines: Theoretical Aspects and Applications
Neural Network World, vol. 2, no. 2, Mar. 1992 (IF later, SJR later) 201–226

J$_3$ V. Beiu: From Systolic Arrays to Neural Networks
Scientific Annals of “Al. I. Cuza” University of Iaşi, vol. 35, no. 4, 1989 (IF later) 375–385

J$_2$ V. Ivanov and V. Beiu
Search Algorithm for an Inference Machine: Software and Hardware
UPB Scientific Bulletin, Control & Computers, vol. AC-50, 1988 (SJR later) 83–96

J$_1$ E. Oltean and V. Beiu
Numerical Aspects in the Implementation of Self-Tuning Algorithms
UPB Scientific Bulletin, Control & Computers, vol. AC-48, 1986 (SJR later) 79–92

CONFERENCES (PEER-REVIEWED) 28 INVITED AND 8 BEST PAPER AWARDS 225

- V. Beiu: Why the Brain Can and Silicon Can't – The Energy Conundrum In progress
- V. Beiu: Why Neural Energy/Power Is So Elusive In progress
- M. Tache et al.: From Trust (Reliable) to Dust (Silicon Chips) – Bridging the Network-Circuit Divide In progress

2023 1

C$_{225}$ P. Poulin, S.R. Cowell, and V. Beiu
Two-Terminal Reliability of the K$_4$-Ladder—Revisited
International Conference on Mathematical Modeling in Physical Sciences IC-MSQUARE 2023
Belgrade, Serbia, August 28-31, 2023, Springer Proc. Maths. & Statistics, vol. 446, May 2024 195–209
https://doi.org/10.1007/978-3-031-52965-8_16

2022 8

C$_{224}$ R.-M. Beiu, V. Dragoi, and V. Beiu
3D Hammocks for Communications
International Workshop on Soft Computing Applications SOFA2022
Arad, Romania, November 21-23, 2022 Pending
https://doi.org/pending

C$_{223}$ R.-M. Beiu, S. Hoara, and V. Beiu
Quantum Is Making Hammocks Ubiquitous
International Workshop on Soft Computing Applications SOFA2022
Arad, Romania, November 21-23, 2022 Pending
https://doi.org/pending

C$_{222}$ M. Tache, V. Dragoi, and V. Beiu
On Low Power Redundant Schemes
International Workshop on Soft Computing Applications SOFA2022
Arad, Romania, November 21-23, 2022 Pending
https://doi.org/pending

C$_{221}$ A.-C. Beiu, R.-M. Beiu, and V. Beiu
Optimal Design of Linear Consecutive Systems
ACM Intl. Conf. Nanoscale Computing & Communication NanoCom2022
Barcelona, Spain, October 05-07, 2022 art. 24
https://doi.org/10.1145/3558583.3558863
https://doi.org/10.54985/peeref.2303p3503376

C$_{220}$ M. Tache, S. Hoara, V. Dragoi, and V. Beiu
Green AI from Kirchhoff to Shannon
International Conference on Computers Communications and Control ICCCC2022
Baile Felix, Romania, May 16-20, 2022 (Chp. 37, Springer AISC vol. 1435, 2023) 433–443
https://doi.org/10.1007/978-3-031-16684-6_37

C$_{219}$ M. Jianu, L. Daus, S. Hoara, and V. Beiu
Using Delta-Wye Transformations for Estimating Network's Reliability
International Conference on Computers Communications and Control ICCCC2022
Baile Felix, Romania, May 16-20, 2022 (Chp. 35, Springer AISC vol. 1435, 2023) 415–426
https://doi.org/10.1007/978-3-031-16684-6_35

C$_{218}$ L. Daus, V. Dragoi, M. Jianu, D. Bucerzan, and V. Beiu
On the Roots of Certain Reliability Polynomials
International Conference on Computers Communications and Control ICCCC2022
Baile Felix, Romania, May 16-20, 2022 (Chp. 34, Springer AISC vol. 1435, 2023) 401–414
https://doi.org/10.1007/978-3-031-16684-6_34

C$_{217}$ V. Beiu, S. Hoara, and R.-M. Beiu
Bridging Reliability to Efficiency – Consecutive Elegant and Simple Design
International Conference on Computers Communications and Control ICCCC2022
Baile Felix, Romania, May 16-20, 2022 (Chp. 33, Springer AISC vol. 1435, 2023) 387–400
https://doi.org/10.1007/978-3-031-16684-6_33

2021 *1*

C$_{216}$ V. Beiu: The Unfolding Road from Dust to Trust ***Invited***$_{28}$
SPIE International Conference "Advances in 3OM: Opto-Mechatronics,
Opto-Mechanics and Optical Metrology" (Adv3OM 2021)
Timisoara, Romania, December 13-16, 2021 (SPIE vol. 12170, May 2022) 1217007(1–7)
https://doi.org/10.1117/12.2601821

2020 *8*

C$_{215}$ V. Beiu, V. Dragoi, and R.-M. Beiu
Why Reliability for Computing Needs Rethinking
IEEE International Conference on Rebooting Computing ICRC 2020, December 1-3, 2020 16–25
https://doi.org/10.1109/ICRC2020.2020.00006
Mentioned under Selected Articles from IEEE Computer Society Digital Library: *"The significance of noise in communications theory is long-established, but similar issues have not generally been considered for computing systems. However, looking to the future, computation will depend on large numbers of nanoscale devices and networks with varying degrees of unreliability. The authors present a unified theory of reliability in future computational networks."* (IEEE Rebooting Computing Highlights, May 2021)

C_{214} V. Dragoi and V. Beiu
Consecutive Systems Asymptotic Threshold Behaviors
International Workshop on Soft Computing Applications SOFA2020
Virtual conference, November 27-29, 2020 (Springer, AISC vol. 1438, 2023) 691–701
https://doi.org/10.1007/978-3-031-23636-5_53

C_{213} L. Daus, M. Jianu, R.-M. Beiu, and V. Beiu
A Tale of Catalan Triangles – Counting Lattice Paths
International Workshop on Soft Computing Applications SOFA2020
Virtual conference, November 27-29, 2020 (Springer, AISC vol. 1438, 2023) 677–690
https://doi.org/10.1007/978-3-031-23636-5_52

C_{212} M. Nagy, V. Dragoi, and V. Beiu
Employing Sorting Nets for Designing Reliable Computing Nets
IEEE Intl. Conf. Nanotech. IEEE-NANO 2020, Virtual, July 29-31, 2020 370–375
https://doi.org/10.1109/NANO47656.2020.9183395

C_{211} S.R. Cowell, S. Hoara, and V. Beiu
Experimenting with Beta Distributions for Approximating Hammocks' Reliability ***Best***
International Conference on Computers Communications and Control ICCCC2020 ***Paper***
Virtual conference, May 11-15, 2020 ***Award***[8]
In I. Dzitac et al. (Eds.): ICCCC 2020, Springer AISC 1243, 2021 70–81
https://doi.org/10.1007/978-3-030-53651-0_6

C_{210} S. Hoara, R.-M. Beiu, and V. Beiu
Investigating Hammock Networks on IBM Q
International Conference on Computers Communications and Control ICCCC2020
Virtual conference, May 11-15, 2020
In I. Dzitac et al. (Eds.): ICCCC2020, Springer AISC 1243, 2021 57–69
https://doi.org/10.1007/978-3-030-53651-0_5

C_{209} S.R. Cowell, M. Nagy, and V. Beiu
Reliability of Two-Terminal Networks Equivalent to Small Optimal Sorting Nets
International Conference on Computers Communications and Control ICCCC2020
Virtual conference, May 11-15, 2020
In I. Dzitac et al. (Eds.): ICCCC 2020, Springer AISC 1243, 2021 45–56
https://doi.org/10.1007/978-3-030-53651-0_4

C_{208} V. Dragoi, S.R. Cowell, and V. Beiu
Tight Bounds on the Coefficients of Consecutive k-out-of-n:F Systems
International Conference on Computers Communications and Control ICCCC2020
Virtual conference, May 11-15, 2020
In I. Dzitac et al. (Eds.): ICCCC 2020, Springer AISC 1243, 2021 35–44
https://doi.org/10.1007/978-3-030-53651-0_3

2018 ***11***

C_{207} V. Dragoi, V. Beiu, and D. Bucerzan
Vulnerabilities of the McEliece Variants Based on Polar Codes
International Conference on Security for Information Technology & Communications SecICT'18
Bucharest, Romania, November 08-09, 2018
In J.-L. Lanet and C. Toma (Eds.): SecITC 2018, Springer, LNCS 11359, 2019 376–390
https://doi.org/10.1007/978-3-030-12942-2_29

C$_{206}$ V. Beiu, S.R. Cowell, and V. Dragoi
The Posets for Reliability: How Fine Can They Be?
International Workshop on Soft Computing Applications SOFA'18
Arad, Romania, September 13-15, 2018
In V.E. Balas et al. (Eds.): SOFA 2018, Springer, AISC 1221, 2021 115–129
https://doi.org/10.1007/978-3-030-51992-6_10

C$_{205}$ V. Dragoi, S.R. Cowell, and V. Beiu
Ordering Series and Parallel Compositions
IEEE International Conference on Nanotechnology IEEE-NANO'18
Cork, Ireland, July 23-26, 2018 8626408(1–4)
https://doi.org/10.1109/NANO.2018.8626408

C$_{204}$ S.R. Cowell, V. Dragoi, N.-C. Rohatinovici, and V. Beiu
Effective Conductances of Moore-Shannon Hammocks
IEEE International Conference on Nanotechnology IEEE-NANO'18
Cork, Ireland, July 23-26, 2018 8626295(1–4)
https://doi.org/10.1109/NANO.2018.8626295

C$_{203}$ V. Dragoi, S.R. Cowell, M. Nagy, and V. Beiu
Matchstick Minimal Circuits
International Symposium Research and Education in an Innovation Era ISREIE'18
Arad, Romania, May 17-20, 2018 (ISSN 2065-2569) 112–121
https://uav.ro/en/conferences/isreie-2018

C$_{202}$ R.-M. Beiu, V.-F. Duma, and V. Beiu
The Latest on the Axon Initial Segment
IEEE International Conference on Computers Communications and Control ICCCC'18
Baile Felix/Oradea, Romania, May 08-12, 2018 136–141
https://doi.org/10.1109/ICCCC.2018.8390450

C$_{201}$ N.-C. Rohatinovici, S.R. Cowell, L. Daus, P. Poulin, V. Dragoi, V.E. Balas, and V. Beiu
On Algorithms for Evaluating the Reliability of Large Hammock Networks
IEEE International Conference on Computers Communications and Control ICCCC'18
Baile Felix/Oradea, Romania, May 08-12, 2018 131–135
https://doi.org/10.1109/ICCCC.2018.8390449

C$_{200}$ V. Dragoi, S.R. Cowell, S. Hoara, P. Gaspar, and V. Beiu
Can Series and Parallel Compositions Improve on Hammocks? ***Best***
IEEE International Conference on Computers Communications and Control ICCCC'18 ***Paper***
Baile Felix/Oradea, Romania, May 08-12, 2018 ***Award***[7] 124–130
https://doi.org/10.1109/ICCCC.2018.8390448

C$_{199}$ V. Beiu, S.R. Cowell, V. Dragoi, S. Hoara, and P. Gaspar
Hammocks versus Hammock
IEEE International Conference on Computers Communications and Control ICCCC'18
Baile Felix/Oradea, Romania, May 08-12, 2018 119–123
https://doi.org/10.1109/ICCCC.2018.8390447

C$_{198}$ M. Nagy, S.R. Cowell, and V. Beiu
Are 3D Fibonacci Spirals for Real? — From Science to Arts and Back to Science
IEEE International Conference on Computers Communications and Control ICCCC'18
Baile Felix/Oradea, Romania, May 08-12, 2018 91–96
https://doi.org/10.1109/ICCCC.2018.8390443

C$_{197}$ R.-M. Beiu, V. Beiu, and V.-F. Duma
Ultra-small Mechanical Deformation Sensor
Using a Hybrid Fiber Optic-based Triangular Photonic Crystal Structure
SPIE Photonics Europe 2018 (SPIE Vol. 10678)
Strasbourg, France, April 22-26, 2018 106780Z(1–6)
https://doi.org/10.1117/12.2307017

2017 ***6***

C$_{196}$ S.R. Cowell, V. Beiu, L. Daus, and P. Poulin
On Cylindrical Hammock Networks
IEEE International Conference on Nanotechnology IEEE-NANO'17
Pittsburgh, USA, July 25-28, 2017 185–188
https://doi.org/10.1109/NANO.2017.8117498

C$_{195}$ R.-M. Beiu, V.-F. Duma, and V. Beiu
Transverse 2D Photonic Crystal Inside a Fiber Optic for Picometer-scale Measurements
IEEE International Conference on Numerical Simulation of Optoelectronic Devices NOSUD'17
Copenhagen, Denmark, July 24-28, 2017 53–54
https://doi.org/10.1109/NUSOD.2017.8009987

C$_{194}$ V. Beiu: Photonic Techniques for Brain Imaging ***Invited***$_{27}$
SPIE-SRLS International Conference for Lasers in Medicine ICLM'17
Timisoara, Romania, July 13-15, 2017 108310I(1–4)
https://doi.org/10.1117/12.2282763

C$_{193}$ R.-M. Beiu, V. Beiu, and V.-F. Duma
Fundamentals and biomedical applications of photonic crystals: An overview
SPIE-SRLS International Conference for Lasers in Medicine ICLM'17
Timisoara, Romania, July 13-15, 2017 108310R(1–5)
https://doi.org/10.1117/12.2282019

C$_{192}$ V. Beiu, L. Daus, N.C. Rohatinovici, and V.E. Balas
Transport Reliability on Axonal Cytoskeleton
IEEE International Conference on Engineering of Modern Electric Systems EMES'17
Oradea, Romania, June 1-2, 2017 160–163
https://doi.org/10.1109/EMES.2017.7980404

C$_{191}$ S.R. Cowell, V. Beiu, L. Daus, and P. Poulin
On Hammock Networks – Sixty Years After
IEEE International Conference on Design & Technology of Integrated Systems in
Nanoscale Era DTIS'17, Palma de Mallorca, Spain, April 4-6, 2017 7929871(1–6)
https://doi.org/10.1109/DTIS.2017.7929871

2016 ***1***

C$_{190}$ R. Toderean (Aldea), O. Geman, I. Chiuchisan, V.E. Balas, and V. Beiu
Novel Method for Neurodegenerative Disorders Screening Patients using
Hurst Coefficients on EEG Delta Rhythm
IEEE International Workshop on Soft Computing Applications SOFA'16
Arad, Romania, August 24-26, 2016
In V.E. Balaş, L.C. Jain, and M.M. Balaş (eds.), Soft Computing Applications, Springer, 2018 349–358
https://doi.org/10.1007/978-3-319-62521-8_29

2015 *6*

C_{189} V. Beiu and M. Tache
Revisiting Delay Variations Statistically Through an Example
IEEE International Semiconductor Conference CAS’15
Sinaia, Romania, October 12-14, 2015 179–182
https://doi.org/10.1109/SMICND.2015.7355200

C_{188} V. Beiu and M. Tache
On Using Schmitt Trigger for Digital Logic
IEEE International Semiconductor Conference CAS’15
Sinaia, Romania, October 12-14, 2015 197–200
https://doi.org/10.1109/SMICND.2015.7355206

C_{187} V. Beiu and L. Daus
Reliability Schemes for Nano-Communications
IEEE European Conference on Circuit Theory and Design ECCTD’15
Trondheim, Norway, August 24-26, 2015 7300038(1–4)
https://doi.org/10.1109/ECCTD.2015.7300038

C_{186} V. Beiu and M. Tache
Statistical Analysis of Static Noise Margins
IEEE European Conference on Circuit Theory and Design ECCTD’15
Trondheim, Norway, August 24-26, 2015 7300090(1–4)
https://doi.org/10.1109/ECCTD.2015.7300090

C_{185} V. Beiu and L. Daus
On 2-Dimensional Consecutive Systems Once Again
IEEE International Conference on Nanotechnology IEEE-NANO’15
Rome, Italy, July 27-30, 2015 464–467
https://doi.org/10.1109/NANO.2015.7388638

C_{184} V. Beiu, W. Ibrahim, M. Tache and F. Kharbash
When One Should Consider Schmitt Trigger Gates
IEEE International Conference on Nanotechnology IEEE-NANO’15
Rome, Italy, July 27-30, 2015 682–685
https://doi.org/10.1109/NANO.2015.7388698

2014 *9*

C_{183} M. Tache, V. Beiu, and T.-J. King Liu
Why Hybridize NEMS with CMOS?
IEEE International Conference on Electronics Circuits and Systems ICECS’14
Marseille, France, December 7-10, 2014 646–649
https://doi.org/10.1109/ICECS.2014.7050068

C_{182} V. Beiu and L. Daus
Deciphering the Reliability Scheme of the Neurons – One Ion Channel at a Time ***Invited***$_{26}$
International Conference on Bio-inspired Info & Communication Technology BICT’14
Boston, MA, USA, December 1-3, 2014 182–187
https://doi.org/10.4108/icst.bict.2014.257905

C_{181} V. Beiu and L. Daus
Why Should We Care About Bounds – Consecutive Systems Revisited
IEEE International Conference on Innovations in Information Technology IIT'14
Al Ain, UAE, November 9-11, 2014 65–70
https://doi.org/10.1109/INNOVATIONS.2014.6987563

C_{180} M. Tache, F. Kharbash, and V. Beiu
On SRAM Bit-Cells Once Again
IEEE International Conference on Innovations in Information Technology IIT'14
Al Ain, UAE, November 9-11, 2014 80–83
https://doi.org/10.1109/INNOVATIONS.2014.6987566

C_{179} M. Tache, V. Beiu, and T.-J. King Liu
A Dual-Voltage Hybrid NEMS-CMOS Low Power Scheme
IEEE International Semiconductor Conference CAS'14
Sinaia, Romania, October 13-15, 2014 211–214
https://doi.org/10.1109/SMICND.2014.6966438

C_{178} V. Beiu, M. Tache, and F. Kharbash
Reliability Enhanced SRAM Bit-Cells
IEEE International Semiconductor Conference CAS'14
Sinaia, Romania, October 13-15, 2014 229–232
https://doi.org/10.1109/SMICND.2014.6966444

C_{177} V. Beiu, W. Ibrahim, M. Tache, and T.-J. King Liu
On Ultra-Low Power Hybrid NEMS-CMOS
IEEE International Conference on Nanotechnology IEEE-NANO'14
Toronto, ON, Canada, August 18-21, 2014 201–206
https://doi.org/10.1109/NANO.2014.6968045

C_{176} V. Beiu and L. Daus
Review of Reliability Bounds for Consecutive-*k*-out-of-*n* Systems
IEEE International Conference on Nanotechnology IEEE-NANO'14
Toronto, ON, Canada, August 18-21, 2014 302–307
https://doi.org/10.1109/NANO.2014.6968048

C_{175} M. Al Kaabi, A. Al Ali, H. Al Janahi, M. Al Kendi, M. Tache, and V. Beiu
Ultra-low Power SRAM Cells with Unconventional Sizing
IEEE International Conference on Nanotechnology IEEE-NANO'14
Toronto, ON, Canada, August 18-21, 2014 308–313
https://doi.org/10.1109/NANO.2014.6968117

2013 *7*

C_{174} F. Kharbash, V. Beiu, M. Tache, and W. Ibrahim
Using Body Bias when Upsizing Length for Maximizing the SNMs of CMOS Gates
IEEE International Conference on Electronics, Circuits, and Systems ICECS'13
Abu Dhabi, UAE, December 8-11, 2013 409–412
https://doi.org/10.1109/ICECS.2013.6815441

C_{173} W. Ibrahim, V. Beiu, M. Tache, and F. Kharbash
On Schmitt Trigger and Other Inverters
IEEE International Conference on Electronics, Circuits, and Systems ICECS'13
Abu Dhabi, UAE, December 8-11, 2013 29–32
https://doi.org/10.1109/ICECS.2013.6815337

C$_{172}$ D. Arotaritei, V. Beiu, M. Turnea, and M. Rotariu
Probabilistic Gate Matrix for Axon-inspired Communication
IEEE International Conference on E-Health and Bioengineering EHB'13
Iasi, Romania, November 21-23, 2013 6707255(1–4)
https://doi.org/10.1109/EHB.2013.6707255

C$_{171}$ N.V. Acharya, J.L. Raju, A. Kumar, M. Tache, and V. Beiu: Monte Carlo Analysis of the
Static Noise Margins for CMOS Gates in Predictive Technology Models
IEEE GCC Conference and Exhibition, Doha, Qatar, November 17-20, 2013 5–10
https://doi.org/10.1109/IEEEGCC.2013.6705739

C$_{170}$ V. Beiu, M. Tache, W. Ibrahim, F. Kharbash, and M. Alioto
On Upsizing Length and Noise Margins
IEEE International Semiconductor Conference CAS'13
Sinaia, Romania, October 13-16, 2013 219–222
https://doi.org/10.1109/SMICND.2013.6688659

C$_{169}$ V. Beiu, A. Beg, W. Ibrahim, F. Kharbash, and M. Alioto
Enabling Sizing for Enhancing the Static Noise Margins
IEEE International Symposium on Quality in Electronic Design ISQED'13
Santa Clara, CA, USA, March 4-6, 2013 278–285
https://doi.org/10.1109/ISQED.2013.6523623

C$_{168}$ P. Santagati and V Beiu
Will Thermal Noise Affect Nano-Communications?
IEEE International Conference on Communications, Signal Processing,
and their Applications ICCSPA'13, Sharjah, UAE, February 12-14, 2013 6487322(1–4)
https://doi.org/10.1109/ICCSPA.2013.6487322

2012 *5*

C$_{167}$ P. Santagati and V. Beiu: A Mathematical Model for the Analysis of the Johnson-Nyquist
Noise on the Reliability of Nano-Communications
International Conference on Bio-Inspired Models of Network, Information,
and Computing Systems BIONETICS'12, Lugano, Switzerland, December 10-12, 2012
In G.A. Di Caro, and G. Theraulaz (eds.), Springer, LNICST vol. 134, July 2014 49–62
https://doi.org/10.1007/978-3-319-06944-9_4

C$_{166}$ V. Beiu, L. Iordaconiu, A. Beg, W. Ibrahim, and F. Kharbash
Low Power and Highly Reliable Gates Using Arrays of Optimally Sized Transistors
IEEE International Semiconductor Conference CAS'12
Sinaia, Romania, October 15-17, 2012 433–436
https://doi.org/10.1109/SMICND.2012.6400738

C$_{165}$ A. Beg, V. Beiu, and W. Ibrahim
Unconventional Transistor Sizing for Reducing Power Alleviates Threshold Voltage Variations
IEEE International Semiconductor Conference CAS'12
Sinaia, Romania, October 15-17, 2012 429–432
https://doi.org/10.1109/SMICND.2012.6400739

C$_{164}$ V. Beiu, M. Calame, G. Cuniberti, C. Gamrat, Z. Konkoli, D. Vuillaume, G. Wendin, and S. Yitzchaik
Aspects of Computing with Locally Connected Networks
AIP International Conference on Numerical Analysis and Applied Mathematics ICNAAM'12
Kos, Greece, September 19-25, 2012 1875–1879
https://doi.org/10.1063/1.4756547

C_{163} V. Beiu, A. Beg, W. Ibrahim, and F. Kharbash
Towards Ultra-Low Voltage/Power Using Unconventionally Sized Arrays of Transistors
IEEE International Conference on Nanotechnology IEEE-NANO'12
Birmingham, UK, August 20-23, 2012 — 6322071(1–5)
https://doi.org/10.1109/NANO.2012.6322071

2011 *7*

C_{162} V. Beiu, W. Ibrahim, A. Beg, and M. Tache
On Axon-inspired Communications
IEEE European Conference on Circuit Theory and Design ECCTD'11
Linköping, Sweden, August 29-31, 2011 — 789–792
https://doi.org/10.1109/ECCTD.2011.6043841

C_{161} V. Beiu, A. Beg, and W. Ibrahim
Atto-Joule Gates for the Whole Voltage Range — ***Invited***$_{25}$
IEEE International Conference on Nanotechnology IEEE-NANO'11
Portland, OR, USA, August 15-18, 2011 — 1424–1429
https://doi.org/10.1109/NANO.2011.6144399

C_{160} A. Beg and V. Beiu
Ultra Low Power/Energy SET-based Axon-inspired Communication
IEEE International Conference on Nanotechnology IEEE-NANO'11
Portland, OR, USA, August 15-18, 2011 — 1183–1186
https://doi.org/10.1109/NANO.2011.6144563

C_{159} W. Ibrahim, A. Beg, and V. Beiu
Highly Reliable and Low-Power Full Adder Cell
IEEE International Conference on Nanotechnology IEEE-NANO'11
Portland, OR, USA, August 15-18, 2011 — 500–503
https://doi.org/10.1109/NANO.2011.6144434

C_{158} V. Beiu, L. Zhang, W. Ibrahim, and M. Tache
Minimizing Communication Power Using Near-neighbor Axon-inspired Lattices
IEEE International Conference on Nanotechnology IEEE-NANO'11
Portland, OR, USA, August 15-18, 2011 — 426–430
https://doi.org/10.1109/NANO.2011.6144502

C_{157} J.J. Wade, L.J. McDaid, J. Harkin, V. Crunelli, J.A.S. Kelso, and V. Beiu
Exploring Retrograde Signaling via Astrocytes as a Mechanism for Self Repair
IEEE International Joint Conference on Neural Networks IJCNN'11
San Jose, CA, USA, July 31 - August 5, 2011 — 3149–3155
https://doi.org/10.1109/IJCNN.2011.6033638

C_{156} A. Beg, V. Beiu, and W. Ibrahim
Atto Joule CMOS Gates Using Reversed Sizing and W/L Swapping
IEEE International New Circuits and Systems Conference NEWCAS'11
Bordeaux, France, June 26-29, 2011 — 498–501
https://doi.org/10.1109/NEWCAS.2011.5981328

2010 *5*

C_{155} W. Ibrahim, V. Beiu, and A. Beg
On NOR-2 von Neumann Multiplexing
IEEE International Design and Test Workshop IDT'10
Abu Dhabi, UAE, December 14-16, 2010 67–72
https://doi.org/10.1109/IDT.2010.5724410

C_{154} V. Beiu and W. Ibrahim
From Transistor Variations to NAND-2 Multiplexing
IEEE International Conference on Nanotechnology IEEE-NANO'10
Seoul, Korea, August 17-20, 2010 1076–1081
https://doi.org/10.1109/NANO.2010.5697864

C_{153} W. Ibrahim and V. Beiu
Device-Level Reliability of Several Full Adder Cells
IEEE International Conference on Nanotechnology IEEE-NANO'10
Seoul, Korea, August 17-20, 2010 1082–1087
https://doi.org/10.1109/NANO.2010.5697865

C_{152} M.H. Sulieman, V. Beiu, and W. Ibrahim
Low-Power and Highly Reliable Logic Gates: Transistor-level Optimizations
IEEE International Conference on Nanotechnology IEEE-NANO'10
Seoul, Korea, August 17-20, 2010 254–257
https://doi.org/10.1109/NANO.2010.5697892

C_{151} L. Zhang, H. Elsayed, and V. Beiu
A Position-Based Broadcast Relay Approach in Mobile Vehicle-to-Vehicle Network
International Conference on Wireless Networks ICWN'10 (part of WorldComp'10)
Las Vegas, NV, USA, July 12-15, 2010 611–616

2009 *11*

C_{150} W. Ibrahim and V. Beiu
Reliability of NAND-2 CMOS Gates from Threshold Voltage Variations
IEEE International Conference Innovations in Information Technology IIT'09
Al Ain, UAE, December 15-17, 2009 135–139
https://doi.org/10.1109/IIT.2009.5413631

C_{149} V. Beiu, B.A.M. Madappuram, P.M. Kelly, and L.J. McDaid
On Two-layer Hierarchical Networks: How Does the Brain Do This? ***Invited***$_{24}$
International ICST Conference on Nano-Networks Nano-Net'09
Luzern, Switzerland, October 18-20, 2009 231–241
https://doi.org/10.1007/978-3-642-04850-0_31

C_{148} P.M. Kelly, F. Tuffy, V. Beiu, and L.J. McDaid: Reduced Interconnects in Neural
Networks Using a Time Multiplexed Architecture Based on Quantum Devices ***Invited***$_{23}$
International ICST Conference on Nano-Networks Nano-Net'09
Luzern, Switzerland, October 18-20, 2009 242–250
https://doi.org/10.1007/978-3-642-04850-0_32

C_{147} V. Beiu, W. Ibrahim, and R.Z. Makki
On Wires Holding a Handful of Electrons ***Invited***$_{22}$
International ICST Conference on Nano-Networks Nano-Net'09
Luzern, Switzerland, October 18-20, 2009 259–269
https://doi.org/10.1007/978-3-642-04850-0_34

C$_{146}$ W. Ibrahim, and V. Beiu
A Bayesian-based EDA Tool for Nano-Circuits Reliability Calculations ***Invited***$_{21}$
International ICST Conference on Nano-Networks Nano-Net’09
Luzern, Switzerland, October 18-20, 2009 276–284
https://doi.org/10.1007/978-3-642-04850-0_36

C$_{145}$ V. Beiu, B.A.M. Madappuram, P.M. Kelly, and L.J. McDaid
On Brain-inspired Hierarchical Network Topologies
IEEE International Conference on Nanotechnology IEEE-NANO’09
Genoa, Italy, July 26-30, 2009 202–205
https://ieeexplore.ieee.org/document/5394594/

C$_{144}$ W. Ibrahim, V. Beiu, and H. Amer
How Much Input Vectors Affect Nano-Circuit’s Reliability Estimates
IEEE International Conference on Nanotechnology IEEE-NANO’09
Genoa, Italy, July 26-30, 2009 699–702
https://ieeexplore.ieee.org/document/5394482/

C$_{143}$ V. Beiu, W. Ibrahim, and R.Z. Makki
On Wires at Low Electron Densities
IEEE International Conference on Nanotechnology IEEE-NANO’09
Genoa, Italy, July 26-30, 2009 703–706
https://ieeexplore.ieee.org/document/5394862/

C$_{142}$ V. Beiu, and W. Ibrahim
On CMOS Circuit Reliability from the MOSFETs and the Input Vectors
IEEE/IFIP International Conference on Dependable Systems and Networks DSN’09
Estoril, Lisbon, Portugal, June 29 - July 2, 2009
http://www.laas.fr/WDSN09/WDSN09_files/Texts/WDSN09-2-2-Beiu.pdf

C$_{141}$ W. Ibrahim, V. Beiu, and H. Amer
Why Should We Care About Input Vectors?
IEEE International Northeast Workshop on Circuit and Systems NEWCAS’09
Toulouse, France, June 28 - July 1, 2009 5290448(1–4)
https://doi.org/10.1109/NEWCAS.2009.5290448

C$_{140}$ V. Beiu, W. Ibrahim, and R.Z. Makki
On Wires Driven by a Few Electrons
IEEE International Northeast Workshop on Circuit and Systems NEWCAS’09
Toulouse, France, June 28 - July 1, 2009 5290455(1–4)
https://doi.org/10.1109/NEWCAS.2009.5290455

2008 *7*

C$_{139}$ R.-M. Beiu and V. Beiu
Pico Sensors for All Seasons — When Light Performs Its Marvels
IEEE International Conference on Innovations in Information Technology IIT’08
Al Ain, UAE, December 16-18, 2008 116–120
https://doi.org/10.1109/INNOVATIONS.2008.4781727

C$_{138}$ R.-M. Beiu, and V. Beiu
Fiber Optic Mechanical Sensor Based on a Triangular-lattice Photonic Crystal
IEEE International Photonics Global Conference IPGC’08
Singapore, December 8-11, 2008 4781347(1–4)
https://doi.org/10.1109/IPGC.2008.4781347

C$_{137}$ V. Beiu, B.A.M. Madappuram, and M. McGinnity
On Brain-inspired Hybrid Topologies for Nano-architectures — A Rent's Rule Approach
IEEE International Conference on Embedded Computer Systems IC-SAMOS'08
Samos, Greece, July 21-24, 2008 33–40
https://doi.org/10.1109/ICSAMOS.2008.4664844

C$_{136}$ V. Beiu: Electrons Behaving Badly – Quo Vadis Nano-architecure? ***Invited$_{20}$***
International Symposium on Information Electronics Systems IES'08
Sendai, Japan, July 14-15, 2008 24–27
http://www.ecei.tohoku.ac.jp/gcoe/en/sympo/sympo_2nd/invited.html

C$_{135}$ S. Lazarova-Molnar and V. Beiu
Reliability Modeling of Circuits with Multi-State Aging Gates
Modeling & Simulation – Methodology, Tools, Software Applications M&S–MTSA'08
Edinburgh, UK, June 16-19, 2008 43–47

C$_{134}$ B.A.M. Madappuram, V. Beiu, P.M. Kelly, and L.J. McDaid
On Brain-inspired Connectivity and Hybrid Network Topologies
IEEE/ACM International Symposium on Nanoscale Architectures NANOARCH'08
Anaheim, CA, USA, June 8-13, 2008 54–61
https://doi.org/10.1109/NANOARCH.2008.4585792

C$_{133}$ V. Beiu and W. Ibrahim
Does the Brain Really Outperform Rent's Rule?
IEEE International Symposium on Circuits and Systems ISCAS'08
Seattle, WA, USA, May 18-21, 2008 640–643
https://doi.org/10.1109/ISCAS.2008.4541499

2007 *15*

C$_{132}$ W. Ibrahim, V. Beiu, and S. Lazarova-Molnar: Accurate Nano-Circuits Reliability Evaluations
Based on Combining Numerical Simulations with Monte Carlo Ones
IEEE International Design and Test Workshop IDT'07
Cairo, Egypt, December 16-18, 2007 139–144
https://doi.org/10.1109/IDT.2007.4437447

C$_{131}$ S. Lazarova-Molnar, V. Beiu, and W. Ibrahim
Proxels for Reliability Assessment of Future Nano-Architectures
IEEE International Design and Test Workshop IDT'07
Cairo, Egypt, December 16-18, 2007 88–89
https://doi.org/10.1109/IDT.2007.4437435

C$_{130}$ S. Lazarova-Molnar, V. Beiu, and W. Ibrahim
Reliability – The Fourth Optimization Pillar of Nanoelectronics
IEEE International Conference on Signal Processing and Communications ICSPC'07
Dubai, UAE, November 24-27, 2007 73–76
https://doi.org/10.1109/ICSPC.2007.4728258

C$_{129}$ W. Ibrahim and V. Beiu
Why Nano-DSP Will Be Fan-in Constrained
IEEE International Conference on Signal Processing and Communications ICSPC'07
Dubai, UAE, November 24-27, 2007 317–320
https://doi.org/10.1109/ICSPC.2007.4728319

C_{128} V. Beiu, H. Amer, and M. McGinnity
On Global Communications for Nano-Architectures – Brain versus Rent’s Rule ***Invited***$_{19}$
International Conference on Design of Circuits and Integrated Systems DCIS’07
Seville, Spain, November 21-23, 2007 305–310
http://www2.imse-cnm.csic.es/dcis07/

C_{127} W. Ibrahim, V. Beiu, and Y.A. Alkhawwar
On the Reliability of Four Full Adder Cells
IEEE International Conference Innovations in Information Technology IIT’07
Dubai, UAE, November 18-20, 2007 720–724
https://doi.org/10.1109/IIT.2007.4430508

C_{126} R.-M. Beiu, C.D. Stanescu, and V. Beiu
A Novel Microstructured Fiber Optic Sensor for Very Small Deformations
SPIE International Symposium on Optomechatronic Technologies ISOT’07, SPIE vol. 6716
Lausanne, Switzerland, October 8-10, 2007 67160D(1–8)
https://doi.org/10.1117/12.754190

C_{125} R.-M. Beiu, C.D. Stanescu, and V. Beiu
Unique In-Fiber Photonic Crystal Sensor
IEEE International Midwest Symposium on Circuit and Systems MWSCAS’07
Montreal, Canada, August 5-8, 2007 116–119
https://doi.org/10.1109/MWSCAS.2007.4488550

C_{124} R.-M. Beiu, C.D. Stanescu, and V. Beiu
Highly Sensitive Nano-Photonic Embedded Sensors
IEEE International Conference on Nanotechnology IEEE-NANO’07
Hong Kong, China, August 2-5, 2007 737–741
https://doi.org/10.1109/NANO.2007.4601293

C_{123} V. Beiu, W. Ibrahim, and S. Lazarova-Molnar
A Fresh Look at Majority Multiplexing – When Devices Get Into the Picture
IEEE International Conference on Nanotechnology IEEE-NANO’07
Hong Kong, China, August 2-5, 2007 883–888
https://doi.org/10.1109/NANO.2007.4601325

C_{122} S. Lazarova-Molnar, V. Beiu, and W. Ibrahim
A Strategy for Reliability Assessment of Future Nano-Circuits
WSEAS International Conference on Circuits, Systems, Communications, Computers CSCC’07
Agios Nikolaos, Crete, Greece, July 23-28, 2007 60–65
https://dl.acm.org/doi/abs/10.5555/1348610.1348623
https://catalogue.nlg.gr/Record/b.523684/TOC

C_{121} W. Ibrahim and V. Beiu
Long Live Small Fan-in Majority Gates – Their Reign Looks Like Coming!
IEEE International Conference on Application-specific Systems
Architectures and Processors ASAP’07, Montreal, Canada, July 8-11, 2007 278–283
https://doi.org/10.1109/ASAP.2007.4429993

C_{120} V. Beiu, W. Ibrahim, and S. Lazarova-Molnar
What von Neumann Did Not Say About Multiplexing: Beyond Gates Failures – The Gory Details
International Work-Conference on Artificial Neural Networks IWANN’07
San Sebastián, Spain, June 19-22, 2007, Springer LNCS 4507 487–496
https://doi.org/10.1007/978-3-540-73007-1_60

C_{119} V. Beiu: Grand Challenges of Nanoelectronics and Possible Architectural Solutions ***Invited***$_{18}$
IEEE International Symposium on Multiple Valued Logic ISMVL'07
Oslo, Norway, May 14-16, 2007 a(1–7)
https://doi.org/10.1109/ISMVL.2007.27

C_{118} V. Beiu and W. Ibrahim
Why Inverters and Small Fan-in Voters Are the Most Promising Gates
IEEE International Workshop on Post-Binary ULSI Systems ULSIWS'07
Oslo, Norway, May 13, 2007 3–10
http://ismvl07.ifi.uio.no/docs/Program_ULSIWS07.pdf

2006 ***4***

C_{117} V. Beiu, W. Ibrahim, Y.A. Alkhawwar, and M.H. Sulieman
Gate Failures Effectively Shape Multiplexing
IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems DFT'06
Washington, DC, USA, October 2-6, 2006 29–37
https://doi.org/10.1109/DFT.2006.33

C_{116} V. Beiu and M.H. Sulieman
On Practical Multiplexing Issues
IEEE International Conference on Nanotechnology IEEE-NANO'06
Cincinnati, OH, USA, July 16-20, 2006 310–313
https://doi.org/10.1109/NANO.2006.247637

C_{115} M.H. Sulieman and V. Beiu
Multiplexing Schemes for Single Electron Technologies
IEEE International Conference on Computer Systems and Applications AICCSA'06
Sharjah, UAE, March 8-11, 2006 424–428
https://doi.org/10.1109/AICCSA.2006.205125

C_{114} V. Beiu, J. Nyathi, S. Aunet, and M.H. Sulieman
Femto Joule Switching for Nano Electronics
IEEE International Conference on Computer Systems and Applications AICCSA'06
Sharjah, UAE, March 8-11, 2006 415–423
https://doi.org/10.1109/AICCSA.2006.205124

2005 ***7***

C_{113} V. Beiu: The Quest for Practical Redundant Computations ***Invited***$_{17}$
IEEE International Conference on Microelectronics ICM'05
Islamabad, Pakistan, December 13-15, 2005 xix
https://doi.org/10.1109/ICM.2005.1590021

C_{112} S. Aunet, Y. Berg, and V. Beiu
Ultra Low-Power Redundant Logic Based on Majority-3 Gates
IFIP International Conference on VLSI System-on-Chip VLSI-SoC'05
Perth, Australia, October 17-19, 2005 553–558
Springer, IFIP 240, ISBN: 978-0-387-73660-0

C_{111} V. Beiu and A. Zawadzki
On Kolmogorov's Superpositions: Novel Gates and Circuits for Nanoelectronics?
IEEE International Joint Conference on Neural Networks IJCNN'05
Montreal, Canada, July 31 - August 4, 2005 651–656
https://doi.org/10.1109/IJCNN.2005.1555908

C_{110} S. Aunet and V. Beiu
Ultra Low Power Fault Tolerant Neural Inspired CMOS Logic
IEEE International Joint Conference on Neural Networks IJCNN'05
Montreal, Canada, July 31 - August 4, 2005 2843–2848
https://doi.org/10.1109/IJCNN.2005.1556376

C_{109} V. Beiu, S. Aunet, J. Nyathi, R. Rydberg III, and A. Djupdal
On the Advantages of Serial Architectures for Low-Power Reliable Computations
IEEE International Conference on Application-specific Systems,
Architectures and Processors ASAP'05, Samos, Greece, July 23-25, 2005 276–281
https://doi.org/10.1109/ASAP.2005.48

C_{108} V. Beiu, A. Djupdal, and S. Aunet
Ultra Low-Power Neural Inspired Addition – When Serial Might Outperform Parallel Architectures
International Work-Conference on Artificial Neural Networks IWANN'05
Barcelona, Spain, June 8-10, 2005, Springer LNCS 3512 486–493
https://doi.org/10.1007/11494669_60

C_{107} V. Beiu, A. Zawadzki, R. Andonie, and S. Aunet
Using Kolmogorov Inspired Gates for Low Power Nanoelectronics
International Work-Conference on Artificial Neural Networks IWANN'05
Barcelona, Spain, June 8-10, 2005, Springer LNCS 3512 438–445
https://doi.org/10.1007/11494669_54

2004 *10*

C_{106} V. Beiu: A Novel Highly Reliable Low-Power Nano Architecture
When von Neumann Augments Kolmogorov ***Invited***$_{16}$
IEEE International Conference on Application-specific Systems,
Architectures and Processors ASAP'04, Galveston, TX, USA, September 27-29, 2004 167–177
https://doi.org/10.1109/ASAP.2004.1342467

C_{105} V. Beiu, U. Rückert, S. Roy, and J. Nyathi
On Nanoelectronic Architectural Challenges and Solutions
IEEE International Conference on Nanotechnology IEEE-NANO'04
Munich, Germany, August 17-19, 2004 628–631
https://doi.org/10.1109/NANO.2004.1392441

C_{104} M.H. Sulieman and V. Beiu
On Single Electron Technology Full Adders
IEEE International Conference on Nanotechnology IEEE-NANO'04
Munich, Germany, August 17-19, 2004 317–320
https://doi.org/10.1109/NANO.2004.1392337

C_{103} S. Roy and V. Beiu
Multiplexing Schemes for Cost-Effective Fault-Tolerance
IEEE International Conference on Nanotechnology IEEE-NANO'04
Munich, Germany, August 17-19, 2004 589–592
https://doi.org/10.1109/NANO.2004.1392429

C_{102} M.H. Sulieman and V. Beiu
Design and Analysis of SET Circuits – Using MATLAB Modules and Simon
IEEE International Conference on Nanotechnology IEEE-NANO'04
Munich, Germany, August 17-19, 2004 618–621
https://doi.org/10.1109/NANO.2004.1392438

C_{101} J. Nyathi, V. Beiu, S. Tatapudi, and D.J. Betwoski
A Charge Recycling Differential Noise-Immune Perceptron
IEEE International Joint Conference on Neural Networks IJCNN'04
Budapest, Hungary, July 25-29, 2004 1995–2000
http://doi.org/10.1109/IJCNN.2004.1380921

C_{100} D.J. Betowski, D. Dwyer, and V. Beiu
A Novel Segmented Parabolic Sine Approximation for Direct Digital Frequency Synthesizers
International Multiconference VLSI'04, Las Vegas, NV, USA, June 21-25, 2004 523–529
https://dblp.uni-trier.de/db/conf/csreaESA/csreaESA2004.html

C_{99} V. Beiu and M.H. Sulieman
Optimal Practical Perceptron Addition – Application to Single Electron Technology
International Multiconference VLSI'04, Las Vegas, NV, USA, June 21-25, 2004 541–547
https://dblp.uni-trier.de/db/conf/csreaESA/csreaESA2004.html

C_{98} M.H. Sulieman and V. Beiu
Characterization of a 16-bit Threshold Logic Single Electron Technology Adder
IEEE International Symposium on Circuits and Systems ISCAS'04
Vancouver, Canada, May 23-26, 2004 681–684
https://doi.org/10.1109/ISCAS.2004.1328838

C_{97} M.H. Sulieman and V. Beiu
On the Design of Multibit SET Adders
NSTI Nanotechnology NanoTech'04, Boston, MA, USA, March 7-11, 2004, vol. 3 169–172
https://www.nsti.org/Nanotech2004/showabstract.html?absno=226

2003 ***17***

C_{96} V. Beiu: Threshold Logic Implementations – The Early Days
IEEE International Midwest Symposium on Circuit and Systems MWSCAS'03
Cairo, Egypt, December 27-30, 2003 1379–1383
https://doi.org/10.1109/MWSCAS.2003.1562552

C_{95} V. Beiu, D.J. Betowski, and P.-S. Wu
Over 100 dBc ROM-less Piecewise Non-linear Direct Digital Frequency Synthesizers
IEEE International Midwest Symposium on Circuit and Systems MWSCAS'03
Cairo, Egypt, December 27-30, 2003 760–763
https://doi.org/10.1109/MWSCAS.2003.1562397

C_{94} V. Beiu, J.M. Quintana, M.J. Avedillo, and M.H. Sulieman
Threshold Logic – From Vacuum Tubes to Nanoelectronics ***Invited***$_{15}$
IEEE International Midwest Symposium on Circuit and Systems MWSCAS'03
Cairo, Egypt, December 27-30, 2003 930–935
https://doi.org/10.1109/MWSCAS.2003.1562439

C_{93} M.H. Sulieman and V. Beiu
Review of Recent Full Adders Implemented in Single Electron Technology ***Invited***$_{14}$
IEEE International Midwest Symposium on Circuit and Systems MWSCAS'03
Cairo, Egypt, December 27-30, 2003 872–875
https://doi.org/10.1109/MWSCAS.2003.1562425

C$_{92}$ P.-S. Wu and V. Beiu
On Accurate Piecewise Linear ROM-less Direct Digital Frequency Synthesizers
IEEE International Conference on Neural Networks and Signal Processing ICNNSP'03
Nanjing, China, December 14-17, 2003 1595–1599
https://doi.org/10.1109/ICNNSP.2003.1281185

C$_{91}$ M.H. Sulieman and V. Beiu
Optimal Practical Adders Using Perceptrons
IEEE International Conference on Neural Networks and Signal Processing ICNNSP'03
Nanjing, China, December 14-17, 2003 345–348
https://doi.org/10.1109/ICNNSP.2003.1279280

C$_{90}$ D.J. Betowski and V. Beiu
Considerations for Phase Accumulator Design for Direct Digital Frequency Synthesizers
IEEE International Conference on Neural Networks and Signal Processing ICNNSP'03
Nanjing, China, December 14-17, 2003 176–179
http://doi.org/10.1109/ICNNSP.2003.1279240

C$_{89}$ R. Andonie, L. Sasu, and V. Beiu
Fuzzy ARTMAP with Relevance Factor
IEEE International Joint Conference on Neural Networks IJCNN'03
Portland, OR, USA, July 20-24, 2003 1975–1980
https://doi.org/10.1109/IJCNN.2003.1223710

C$_{88}$ V. Beiu: A Survey of Perceptron Circuit Complexity Results
IEEE International Joint Conference on Neural Networks IJCNN'03
Portland, OR, USA, July 20-24, 2003 989–994
http://doi.org/10.1109/IJCNN.2003.1223825

C$_{87}$ V. Beiu, J.M. Quintana, M.J. Avedillo, and R. Andonie
Differential Implementations of Threshold Logic Gates
IEEE International Symposium on Signal, Circuits and Systems SCS'03
Iaşi, Romania, July 10-11, 2003 489–492
https://doi.org/10.1109/SCS.2003.1227096

C$_{86}$ Z. Zhou, D.J. Betwoski, X. Li, G. La Rue, and V. Beiu
High Performance Direct Digital Frequency Synthesizers
Biennial University/Government/Industry Microelectronics Symposium UGIM'03
Boise, ID, USA, June 30 - July 2, 2003 368–369
https://doi.org/10.1109/UGIM.2003.1225770

C$_{85}$ V. Beiu: Constructive Threshold Logic Addition – A Synopsis of the Last Decade
International Conference on Artificial Neural Networks ICANN'03
Istanbul, Turkey, June 26-29, 2003, Springer LNCS 2714 745–752
https://doi.org/10.1007/3-540-44989-2_89

C$_{84}$ V. Beiu, J.M. Quintana, and M.J. Avedillo
Review of Capacitive Threshold Gate Implementations
International Conference on Artificial Neural Networks ICANN'03
Istanbul, Turkey, June 26-29, 2003, Springer LNCS 2714 737–744
https://doi.org/10.1007/3-540-44989-2_88

C$_{83}$ S. Tatapudi and V. Beiu
Split-Precharge Differential Noise-Immune Threshold Logic Gate
International Work-Conference on Artificial Neural Networks IWANN'03
Menorca, Spain, June 3-6, 2003, Springer LNCS 2687 49–56
https://doi.org/10.1007/3-540-44869-1_7

C_{82} R. Andonie, L.M. Sasu, and V. Beiu
A Modified Fuzzy ARTMAP Architecture for Incremental Learning Function Approximation
International Conference on Neural Networks and Computational Intelligence NCI'03
Cancun, Mexico, May 19-21, 2003, ACTA Press 124–129
http://www.actapress.com/Abstract.aspx?paperId=13609

C_{81} V. Beiu: On Existential and Constructive Neural Complexity Results
International Conference on Neural Networks and Computational Intelligence NCI'03
Cancun, Mexico, May 19-21, 2003, ACTA Press 63–72
http://www.actapress.com/Abstract.aspx?paperId=13599

C_{80} V. Beiu, J.M. Quintana, and M.J. Avedillo
Review of Differential Threshold Gate Implementations
International Conference on Neural Networks and Computational Intelligence NCI'03
Cancun, Mexico, May 19-21, 2003, ACTA Press 44–49
http://www.actapress.com/Abstract.aspx?paperId=13596

2002 *2*

C_{79} V. Beiu: On the Node Complexity of Threshold Gate Circuits with Sub-Linear Fan-Ins
International Conference on Neural Networks and Soft Computing ICNNSC'02
Zakopane, Poland, June 11-15, 2002, Springer, Advances in Soft Computing vol. 19 143–148
https://doi.org/10.1007/978-3-7908-1902-1_18

C_{78} V. Beiu: Depth-Size Tradeoffs for Threshold Gate Circuits
Italian Workshop on Neural Networks WIRN-Vietri'02
Vietri sul Mare, Italy, May 31 - June 1, 2002 88–91

2001 *2*

C_{77} V. Beiu: On Higher Order Noise Immune Perceptrons
IEEE International Joint Conference on Neural Networks IJCNN'01
Washington, DC, USA, July 14-19, 2001, vol. 1 246–251
https://doi.org/10.1109/IJCNN.2001.939025

C_{76} V. Beiu: On VLSI-Optimal Neural Computations
International Conference on Control Systems and Computer Science CSCS-13
Bucharest, Romania, May 31 - June 3, 2001 450–455

2000 *2*

C_{75} V. Beiu: High-Speed Noise Robust Threshold Gates ***Best Paper Award***[6]
IEEE International Semiconductor Conference CAS'00
Sinaia, Romania, October 10-14, 2000, vol. 1 79–82
https://doi.org/10.1109/SMICND.2000.890191

C_{74} V. Beiu: Ultra-Fast Noise Immune CMOS Threshold Gates
IEEE Midwest Symposium on Circuits and Systems MWSCAS'00
Lansing, MI, USA, August 8-11, 2000, vol. 3 1310–1313
https://doi.org/10.1109/MWSCAS.2000.951456

1999 **1**

C_{73} V. Beiu: Neural Addition and Fibonacci Numbers
International Work-Conference on Artificial Neural Networks IWANN'99
Alicante, Spain, June 2-4, 1999, Springer LNCS 1607 198–207
https://doi.org/10.1007/BFb0100486

1998 **10**

C_{72} V. Beiu: On Kolmogorov's Superposition and Boolean Functions
IEEE Brazilian Symposium on Neural Networks SBRN'98
Belo Horizonte, Brazil, December 9-11, 1998 55–60
http://doi.org/10.1109/SBRN.1998.730994

C_{71} V. Beiu: Larger Bases and Mixed Analog/Digital Neural Networks
International Conference on Artificial Neural Networks in Engineering ANNIE'98
St. Louis, MI, USA, November 1-4, 1998. In C.H. Dagli et al. (Eds.), ASME Press 63–70

C_{70} V. Beiu: 2D Neural Hardware vs 3D Biological Ones **Invited$_{13}$**
ICSC/IFAC International Symposium on Neural Computations NC'98
Vienna, Austria, September 23-25, 1998, ICSC Academic Press 37–45
http://www.icsc.ab.ca/publications/list_nc98.html

C_{69} V. Beiu: On Automatic Synthesis of Analog/Digital Circuits
International Symposium on Nonlinear Theory and Its Applications NOLTA'98
Crans-Montana, Switzerland, September 14-17, 1998, vol. 2 799–802

C_{68} V. Beiu and K.R. Moore
On Analog Implementation of Discrete Neural Networks
International Workshop on Fuzzy Logic and Intelligent Technologies FLINS'98
Antwerp, Belgium, September 14-16, 1998, World Scientific (ISBN: 981-02-3532-1) 258–265

C_{67} V. Beiu: Implementing Size-Optimal Discrete Neural Networks Requires Analog Circuitry
European Signal Processing Conference EuSiPCo'98
Rhodes, Greece, September 8-11, vol. 3, Typorama (ISBN: 978-960-7620-06-4) 1325–1328

C_{66} V. Beiu: Neural Inspired Parallel Computations Require Analog Processors **Invited$_{12}$**
International Conference on Parallel Computing and Electrical Engineering PARELEC'98
Bialystok, Poland, September 2-5, 1998 39–53

C_{65} V. Beiu and H.E. Makaruk
Small Fan-In Is Beautiful
IEEE International Joint Conference on Neural Networks IJCNN'98
Anchorage, AK, USA, May 4-9, 1998, vol. 2 1321–1326
https://doi.org/10.1109/IJCNN.1998.685966

C_{64} V. Beiu: How to Build VLSI-Efficient Neural Chips **Invited$_{11}$**
ICSC International Symposium on Engineering of Intelligent Systems EIS'98
Tenerife, Canary Islands, Spain, February 9-13, 1998, ICSC Academic Press, vol. 2 66–75
http://www.icsc.ab.ca/publications/list_eis98.html

C_{63} V. Beiu and H.E. Makaruk **Invited$_{10}$**
Deeper and Sparser Nets Are Optimal
ICSC International Symposium on Engineering of Intelligent Systems EIS'98
Tenerife, Canary Islands, Spain, February 9-13, 1998, ICSC Academic Press, vol. 2 59–65
http://www.icsc.ab.ca/publications/list_eis98.html

1997 *11*

C_{62} V. Beiu, S. Draghici, and H.E. Makaruk
On Limited Fan-in Optimal Neural Networks
IEEE Brazilian Symposium on Neural Networks IV SBRN
Goiania, Brazil, December 3-5, 1997 19–30
https://doi.org/10.1109/SBRN.1997.645844

C_{61} V. Beiu and H.E. Makaruk
Computing Volumes of n-Dimensional Complexes
International Symposium on Nonlinear Theory and Its Applications NOLTA'97
Honolulu, HI, USA, November 29 - December 3, 1997, IEICE Press, vol. 1 417–420

C_{60} S. Draghici, V. Beiu, and I.K. Sethi
A VLSI Optimal Constructive Algorithm
International Conference on Artificial Neural Networks in Engineering ANNIE'97
St. Louis, MI, USA, November 9-12, 1997, ASME Press 145–151

C_{59} V. Beiu: When Reduced Connectivity Neural Networks Are Complexity Optimal?
International Workshop on Neural Networks HELNET'97
Montreux, Switzerland, October 4-6, 1997, VU University Press 109–116

C_{58} V. Beiu and S. Draghici
On Sparsely Connected Optimal Neural Networks
International Conference on Microelectronics for Neural Networks MicroNeuro'97
Dresden, Germany, September 24-26, 1997, Sächsisches Druck- und Verlagshaus 56–63

C_{57} V. Beiu and S. Draghici
Limited Weights Neural Networks – Very Tight Entropy Based Bounds
ICSC International Symposium on Soft Computing SOCO'97
Nîmes, France, September 17-19, 1997, ICSC Academic Press 111–118
http://www.icsc.ab.ca/publications/list_soco97.html

C_{56} V. Beiu: Enhanced Lower Entropy Bounds with Application to Constructive Learning
IEEE EuroMicro-Workshop on Computational Intelligence EuroMicro'97
Budapest, Hungary, September 1-4, 1997 541–548
https://doi.org/10.1109/EURMIC.1997.617371

C_{55} V. Beiu: Optimization of Circuits Using a Constructive Neural Network Learning Algorithm
International Conference on Engineering Applications of Neural Networks EANN'97
Stockholm, Sweden, June 16-18, 1997, Åbo Akademis 291–194

C_{54} V. Beiu and T. De Pauw
Tight Bounds on the Size of Neural Networks for Classification Problems
International Work-Conference on Artificial Neural Networks IWANN'97
Lanzarote, Canary Islands, Spain, June 4-6, 1997, Springer LNCS 1240 743–752
https://doi.org/10.1007/BFb0032533

C_{53} V. Beiu: When Constants Are Important
International Conference on Control System and Computer Science CSCS-11
Bucharest, Romania, May 28-31, 1997, vol. 2 106–111

C_{52} S. Draghici and V. Beiu
Entropy Based Comparison of Neural Networks for Classification
Italian Workshop on Neural Nets WIRN-Vietri'97
Vietri sul Mare, Salerno, Italy, May 22-24, 1997, Springer 124–132
https://doi.org/10.1007/978-1-4471-1520-5_6

1996 *3*

C_{51} V. Beiu: New VLSI Complexity Results for Threshold Gate COMPARISON
Brazilian Symposium on Neural Networks III SBRN
Recife, Brazil, November 12-14, 1996, UFPE-DI 251–258

C_{50} V. Beiu: VLSI Complexity of Threshold Gate COMPARISON ***Invited***$_9$
International Symposium on Neuro-Fuzzy Systems AT’96
Lausanne, Switzerland, August 29-31, 1996, Aati 161–170
https://doi.org/10.1109/ISNFS.1996.603834

C_{49} V. Beiu and J.G. Taylor
Direct Synthesis of Neural Networks
International Conference on Microelectronics for Neural Networks MicroNeuro’96
Lausanne, Switzerland, February 12-14, 1996 257–264
https://doi.org/10.1109/MNNFS.1996.493800

1995 *5*

C_{48} J.C. Lemm, V. Beiu, and J.G. Taylor
Density Estimation as a Preprocessing Step for Constructive Algorithms
Annual Symposium on Neural Network SNN’95
Nijmegen, The Netherlands, September 14-15, 1995, Springer 213–216
https://doi.org/10.1007/978-1-4471-3087-1_41

C_{47} V. Beiu and J.G. Taylor
Optimal Mapping of Neural Networks onto FPGAs
International Workshop on Artificial Neural Networks IWANN’95
Málaga, Spain, June 7-9, 1995, Springer LNCS 930 822–829
https://doi.org/10.1007/3-540-59497-3_256

C_{46} V. Beiu and J.G. Taylor
Area-Efficient Constructive Learning Algorithm ***Invited***$_8$
International Conference on Control System and Computer Science CSCS-10
Bucharest, Romania, May 24-26, 1995, vol. 3 293–310

C_{45} V. Beiu and J.G. Taylor
VLSI Optimal Learning Algorithm
International Conference on Artificial Neural Networks and Genetic
Algorithms ICANNGA’95, Alès, France, April 19-21, 1995, Springer 61–64
https://doi.org/10.1007/978-3-7091-7535-4_18

C_{44} V. Beiu: Optimal VLSI Implementations of Neural Networks, VLSI-Friendly Learning Algorithms ***Invited***$_7$
Applied Decision Technologies Conference ADT’95, London, UK, April 3-5, 1995 193–207

1994 *6*

C_{43} V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins
Addition Using Constrained Threshold Gates ***Invited***$_6$
International Conference on Technical Informatics ConTI’94
Timişoara, Romania, November 16-19, 1994, vol. 5 166–177

C_{42} V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins
Placing Feedforward Neural Networks Among Several Circuit Complexity Classes
World Conference on Neural Networks WCNN’94
San Diego, CA, USA, June 4-9, 1994, Lawrence Erlbaum & INNS (ISBN 0-8058-1745-X) 584–589

C$_{41}$ V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins
On the Circuit Complexity of Feedforward Neural Networks
International Conference on Artificial Neural Networks ICANN'94
Sorrento, Italy, May 26-29, 1994, Springer 521–524
https://doi.org/10.1007/978-1-4471-2097-1_121

C$_{40}$ V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins
Area-Time Performances of Some Neural Computations
International Symposium on Signal Processing, Robotics, & Artificial Neural Networks
SPRANN'94, Lille, France, April 25-27, 1994, GERF EC (ISBN: 2950290833) 664–668

C$_{39}$ V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins
VLSI Complexity Reduction by Piece-Wise Approximation of the Sigmoid Function ***Invited$_5$***
European Symposium on Artificial Neural Networks ESANN'94
Brussels, Belgium, April 20-22, 1994, D facto 181–186
https://www.elen.ucl.ac.be/esann/proceedings/papers.php?ann=1994#ES1994-529

C$_{38}$ V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins
Learning from Examples and VLSI Implementation of Neural Networks ***Invited$_4$***
European Meeting on Cybernetics and System Research EMCSR'94
Vienna, Austria, April 5-8, 1994, World Scientific (ISBN: 9789814534376) 1767–1774

1993 *5*

C$_{37}$ V. Beiu, J.A. Peperstraete, and R. Lauwereins
Enhanced Threshold Gate Fan-In Reduction Algorithms
International Conference for Young Computer Scientists ICYCS'93
Beijing, China, July 15-17, 1993, Tsinghua Press (ISBN: 7-302-00888) 3.39–3.42

C$_{36}$ V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins
Overview of Some Efficient Threshold Gate Decomposition Algorithms ***Invited$_3$***
International Conference on Control System and Computer Science CSCS-9
Bucharest, Romania, May 25-28, 1993, Joint Printing House, vol. 1 458–469

C$_{35}$ D.O. Creteanu, V. Beiu, J.A. Peperstraete, and R. Lauwereins
Systolic Pattern Recognition Based on a Neural Network Algorithm
International Conference on Artificial Neural Networks and Genetic
Algorithms ICANNGA'93, Innsbruck, Austria, April 13-16, 1993, Springer 137–144
https://doi.org/10.1007/978-3-7091-7533-0_22

C$_{34}$ V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins
Efficient Decomposition of Comparison and Its Applications
European Symposium on Artificial Neural Networks ESANN'93
Brussels, Belgium, April 7-9, 1993, D facto 45–50
https://www.elen.ucl.ac.be/esann/proceedings/papers.php?ann=1993#ES1993-507

C$_{33}$ V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins
COMPARISON and Threshold Gate Decomposition
International Conference on Microelectronics for Neural Networks MicroNeuro'93
Edinburgh, UK, April 6-8, 1993, Pub. UnivEd 83–90

1992 *6*

C_{32} V. Beiu, J.A. Peperstraete, and R. Lauwereins
Enhanced Threshold Gate Fan-in Reduction Algorithm ***Invited$_2$***
Interdisciplinary Centrum for Neural Networks ICNN’92
Leuven, Belgium, November 19, 1992, KUL Press 65–70

C_{31} V. Beiu, J.A. Peperstraete, and R. Lauwereins
Simpler Neural Networks by Fan-in Reduction
IEEE International Joint Conference on Neural Networks IJCNN’92
Beijing, China, November 3-6, 1992, vol. 3 204–209

C_{30} V. Beiu, J.A. Peperstraete, and R. Lauwereins
Algorithms for Fan-in Reduction
International Conference on Neural Networks and Their Applications NeuroNimes’92
Nîmes, France, November 2-6, 1992, EC2 589–600

C_{29} V. Beiu, J.A. Peperstraete, and R. Lauwereins
Using Threshold Gates to Implement Sigmoid Nonlinearities
International Conference on Artificial Neural Networks ICANN’92
Brighton, UK, September 4-7, 1992, Elsevier 1447–1450
https://doi.org/10.1016/B978-0-444-89488-5.50133-0

C_{28} V. Beiu, D.C. Ioan, and M.C. Dumbrava
Continuous Boltzmann Machines: Theoretical Aspects and Applications
IEEE European Computer Conference CompEuro’92, Hague, Netherlands, May 4-8, 1992 193–198
https://doi.org.10.1109/CMPEUR.1992.218510

C_{27} V. Beiu, D.C. Ioan, M.C. Dumbrava, and O. Robciuc
Physical Fields Determination Using Continuous Boltzmann Machines
IASTED International Symposium APPLIED INFORMATICS’92
Innsbruck, Austria, February 10-12, 1992, Acta Press 284–287

1991 *3*

C_{26} S. Georgescu and V. Beiu
Optimal Reconstruction from Sampled Data with Parallel Structures
ISMM International Workshop on Parallel Computing ParComp’91
Trani, Italy, September 10-13, 1991, Anaheim: Acta Press (ISBN: 0889861471) 260–263

C_{25} V. Beiu: Neural Network for Digital Image Enhancement
International Conference on Artificial Neural Networks ICANN’91
Espoo, Finland, June 24-28, 1991, Elsevier, vol. 2 1071–1074
https://doi.org/10.1016/B978-0-444-89178-5.50021-X

C_{24} V. Beiu: NeuroSim – A Neural Network Simulator
International Conference on Control System and Computer Science CSCS-8
Bucharest, Romania, May 22-25, 1991 28–36

1990 *1*

C_{23} V. Beiu: Neural Network Priority Queue ***Invited$_1$***
International Workshop on Parallel Processing by Cellular Automata PARCELLA’90
Berlin, Germany, September 19-21, 1990, Akademie Verlag 130–136

1989 4

C_{22} V. Beiu, A. Florea, and S. Georgescu
The Facilities of the NeuroSim Environment
International Symposium on Informatics INFO-IASI’89, Iaşi, Romania, October 19-21, 1989 196–202

C_{21} V. Beiu and S. Georgescu
Recognition of Moving Objects Using NeuroSim
International Symposium on Informatics INFO-IASI’89, Iaşi, Romania, October 19-21, 1989 186–195

C_{20} A. Petrescu and V. Beiu
The “Hello VLSI” CAD Environment
IEEE Annual Conference on Semiconductors CAS’89, Sinaia, Romania, October 11-14, 1989 78–82

C_{19} V. Beiu and S. Georgescu
Consideration of Vision Based on Associative Neural Networks
IEEE Annual European Computer Conference CompEuro’89
Hamburg, Germany, May 8-12, 1989, vol. 2 121–124
https://doi.org/10.1109/CMPEUR.1989.93388

1988 1

C_{18} V. Beiu: VLSI Arrays Implementing Parallel Line-Drawing Algorithms
International Workshop on Parallel Processing by Cellular Automata PARCELLA’88
Berlin, Germany, October 17-21, 1988, Springer LNCS 342 239–247
https://doi.org/10.1007/3-540-50647-0_114

1987 5

C_{17} V. Beiu: A Smart-Memory for Set-Structure Processing
International Symposium on Informatics INFO-IASI’87
Iaşi, Romania, October 8-10, 1987,vol. 1 404–413

C_{16} V. Beiu: VLSI Arrays Implementing Parallel Line-Drawing Algorithms
International Symposium on Informatics INFO-IASI’87
Iaşi, Romania, October 8-10, 1987, vol. 1 395–403

C_{15} V. Beiu: Smart VLSI Memory Chips Implementing Elementary Operations on Lists
International Conference on Control System and Computer Science CSCS-7
Bucharest, Romania, May 27-30, 1987, vol. 3 16–22

C_{14} E. Oltean and V. Beiu
Adaptive Kalman Filtering – Implementation of a Dedicated Structure
International Conference on Control System and Computer Science CSCS-7
Bucharest, Romania, May 27-30, 1987, vol. 2 21–26

C_{13} V. Beiu and C. Constantinescu
Fault-Tolerant Systolic Arrays for Antialiasing
IEEE Annual European Computer Conference CompEuro’87
Hamburg, Germany, May 11-15, 1987 720–723

1986 1

C_{12} V. Beiu: Self-Testable and Self-Repairable Antialiasing Unit
International MICROELECTRONICS’86 Conference
Plovdiv, Bulgaria, October 23–25, 1986, vol. 2 183–195

1985 *4*

C_{11} V. Beiu and A. Neagu
Algorithm for Adding Universal Represented Real (URR) Numbers
International Symposium on Informatics INFO-IASI'85
Iaşi, Romania, October 18-19, 1985, vol. 2 760–768

C_{10} V. Beiu: Dedicated Computing Unit for Antialiasing
International Symposium on Informatics INFO-IASI'85
Iaşi, Romania, October 18-19, 1985, vol. 2 590–599

C_9 V. Beiu and I. Rosu
VLSI Implementation of a Self-Testable Real Content Addressable Memory
International Conference on Control System and Computer Science CSCS-6
Bucharest, Romania, May 22-25, 1985, vol. 2 400–405

C_8 V. Beiu, A. Petrescu, and I. Rosu
Design of Hierarchically Organized Memories for VLSI Implementation
International Conference on Control System and Computer Science CSCS-6
Bucharest, Romania, May 22-25, 1985, vol. 2 69–75

1983 *1*

C_7 I. Rosu, V. Beiu, and T. Kappel
An Algorithm for Priorities Evaluation in a Statistical Multiplexer
International Conference on Control System and Computer Science CSCS-5
Bucharest, Romania, June 8-11, 1983, vol. 2 368–372

1982 *1*

C_6 V. Beiu: High Speed Algorithm for Executing the MOD Instruction
National Conference on Electronics, Telecommunication, Control and Computers CNETAC'82
Bucharest, Romania, November 17-19, 1982 175–179

1980 *3*

C_5 A. Aurelian, V. Beiu, and R. Muntean
Programmable Binary Multipliers in the Range $2^2 : 2^{10}$
Students Scientific Research Conference
Bucharest, Romania, May 17-18, 1980 ***Best Paper Award***$_5$ 721–725

C_4 V. Beiu, R. Muntean, and A. Aurelian
Graphic Workstation – RAM/ROM Character Generator
Students' Scientific Research Conference
Bucharest, Romania, May 17-18, 1980 ***Best Paper Award***$_4$ 726–730

C_3 R. Munteanu, A. Aurelian, and V. Beiu
Ultra High Speed TTL Unit for a Graphic Workstation
Students Scientific Research Conference
Bucharest, Romania, May 17-18, 1980 ***Best Paper Award***$_3$ 731–735

1977 *2*

C_2 V. Beiu: Field Effect Optoelectronic Equipments
Students' Scientific Research Conference
Bucharest, Romania, May 13-14, 1977 ***Best Paper Award***$_2$ 476–480

C_1 V. Beiu: Bistable Cholesteric Mixtures with Positive Dielectric Anisotropy
Students Scientific Research Conference
Bucharest, Romania, May 13-14, 1977
Best Paper Award$_1$ 471–475

OTHER CONFERENCES ***7 INVITED AND 1 BEST PAPER AWARD*** ***53***

O_{53} P. Poulin, S.R. Cowell, and V. Beiu
On the K_4-ladder Two-terminal Reliability Once Again
IEEE Advances in Science & Engineering Technology (ASET)
Dubai, UAE, February 20-23, 2023

O_{52} A.-C. Beiu and V. Beiu
Designing Highly Reliable Systems Using Random Devices
IBM/IEEE CAS/EDS – AI Compute Symposium @ IBM T.J. Watson Research Center
Yorktown Heights, NY, USA, October 12-14, 2022
https://doi.org/10.54985/peeref.2303p1524423

O_{51} R.-M. Beiu, M.M. Balas, V.E. Balas, and V. Beiu
Seeing is Believing
International Summit on Optics, Photonics and Laser Technologies OPTICS&LASERS'19
San Francisco, CA, USA, June 03-05, 2019

O_{50} M. Nagy, S.R. Cowell, and V. Beiu
Optimal Cubic Fibonacci Identities for 3D Packing
International Symposium Research and Education in Innovation Era ISREIE'19
Arad, Romania, May 23-25, 2019

O_{49} M. Tache, S.R. Cowell, and V. Beiu
Turning Sizing on Its Head and More
International Symposium Research and Education in Innovation Era ISREIE'19
Arad, Romania, May 23-25, 2019

O_{48} R.-M. Beiu and V. Beiu
Sidestepping the Bounds of Diffraction
International Symposium Research and Education in Innovation Era ISREIE'19
Arad, Romania, May 23-25, 2019

O_{47} G. Cristescu, V. Dragoi, and V. Beiu
Cubic Spline Approximation of the Reliability Polynomials of Two Dual Hammock Networks
International Symposium Research and Education in Innovation Era ISREIE'19
Arad, Romania, May 23-25, 2019

O_{46} L. Hamad, A. Fahad, A. Saeed, F. Kharbash, and V. Beiu
On Reliability-Enhanced Quantum Cellular Automata (QCA) Designs
UAEU Annual Research & Innovation Conference ARIC'15
Al Ain, UAE, November 24-25, 2015

O_{45} L. Daus and V. Beiu
A Survey of Consecutive-*k*-out-of-*n* Systems Bounds
IEEE International Symposium on Multiple-Valued Logic ISMVL'14
International Workshop on Post-Binary ULSI Systems ULSIWS'14
Bremen, Germany, May 18-21, 2014

O_{44} M. Tache, V. Beiu, W. Ibrahim, F. Kharbash, and M. Alioto
Sizing for Static Noise Margins Revisited
European Workshop on CMOS Variability VARI'13/PATMOS'13
Karlsruhe, Germany, September 9-11, 2013

O$_{43}$ V. Beiu, W. Ibrahim, A. Beg, and M. Tache
On Sizing Transistors for Threshold Voltage Variations
International Workshop on Design for Reliability DFR'12 (in conjunction with HiPEAC'12)
Paris, France, January 23-25, 2012
http://www.cs.ucy.ac.cy/carch/DFR2012/presentations/S2_3.pdf

O$_{42}$ V. Beiu and W. Ibrahim
NAND Multiplexing Down to Nuts and Bolts
International Conference on Ultimate Integration on Silicon ULIS'10
Glasgow, UK, March 17-19, 2010

O$_{41}$ B.A.M. Madappuram, V. Beiu, and T.M. McGinnity
On Brain-inspired Hybrid Network Topologies for Future Nano-architectures ***Best Paper Award***[1]
UAEU Annual Research Conference ARC-9, Al Ain, UAE, April 21-23, 2008

O$_{40}$ S. Lazarova-Molnar and V. Beiu
Mapping the Proxel-Based Method to Reliability Analysis of Nano-architectures
UAEU Annual Research Conference ARC-9, Al Ain, UAE, April 21-23, 2008

O$_{39}$ R.-M. Beiu, C.D. Stanescu, and V. Beiu
Nanostructured Fiber Optics as Highly Sensitive Mechanical Sensors ***Invited***[7]
International Trends in NanoTechnology Conference TNT'07
San Sebastian, Spain, September 3-7, 2007

O$_{38}$ W. Ibrahim and V. Beiu
A Hybrid Monte-Carlo and Numerical Simulations Approach for Future Nano-circuits Reliability Calculation
International Trends in NanoTechnology Conference TNT'07
San Sebastian, Spain, September 3-7, 2007

O$_{37}$ S. Lazarova-Molnar, V. Beiu, and W. Ibrahim
Proxels for Reliability Assessment of Future Nano-Circuits
International Trends in NanoTechnology Conference TNT'07
San Sebastian, Spain, September 3-7, 2007

O$_{36}$ H. Amer and V. Beiu
On Global Communications for Nano-Architectures – Brain versus Rent's Rule
International Trends in NanoTechnology Conference TNT'07
San Sebastian, Spain, September 3-7, 2007

O$_{35}$ B.A.M. Madappuram and V. Beiu
Using Standing Waves for Communications Might Work for Crossbar Architectures
International Trends in NanoTechnology Conference TNT'07
San Sebastian, Spain, September 3-7, 200

O$_{34}$ M.H. Sulieman and V. Beiu
Investigating the Reliability of Single-Electron-Technology Gates and Circuits
UAEU Annual Research Conference ARC-8, Al Ain, UAE, April 23-25, 2007

O$_{33}$ V. Beiu, J. Nyathi, and S. Aunet
Sub-Pico (Femto) Joule Switching: High-Speed Reliable CMOS Circuits Are Feasible
International Conference on Innovations in Information Technology IIT'05
Dubai, UAE, September 26-28, 2005
http://www.it-innovations.ae/iit005/proceedings/articles/E_5_IIT05_Beiu.pdf

O$_{32}$ V. Beiu, S. Aunet, R. Rydberg III, A. Djupdal, and J. Nyathi
The Vanishing Majority Gate – Trading Power and Speed for Reliability
IEEE International Workshop on Design and Test of Defect-Tolerant
Nanoscale Architectures NanoArch'05, Palm Springs, CA, USA, May 1, 2005

O_{31} J. Nyathi, V. Beiu, and S. Aunet
Sub Femto Joule Switching – High Speed Reliable CMOS Circuits Are Feasible
ASILOMAR Conference on Signal, Systems and Computers
Pacific Groove, CA, USA, November 7-10, 2004

O_{30} J. Nyathi, V. Beiu, and S. Aunet
Femto Joule Switching – Review of Low Energy Design Styles for the Nano Era ***Invited***$_6$
International Symposium on Nano and Giga Challenges in Nanoelectronics NGCM’04
Krakow, Poland, September 13-17, 2004

O_{29} V. Beiu, U. Rückert, S. Roy, and J. Nyathi
On Nanoelectronic Architectural Challenges and Plausible Solutions
International Symposium on Nano and Giga Challenges in Nanoelectronics NGCM’04
Krakow, Poland, September 13-17, 2004

O_{28} V. Beiu and A. Zawadzki
Why VLSI/Nano Library Design Should Use Kolmogorov’s Superpositions
International Symposium on Nano and Giga Challenges in Nanoelectronics NGCM’04
Krakow, Poland, September 13-17, 2004

O_{27} V. Beiu: On Biological and Hardware Neural Networks ***Invited***$_5$
International Joint Meeting AMS-SMM, Denton, TX, USA, May 19-22, 1999

O_{26} V. Beiu, J. Frigo, and K.R. Moore
Why the Nervous Networks Are Reliable
International Symposium on Artificial Intelligence and Adaptive Systems CIMAF’99
Havana, Cuba, March 24-28, 1999

O_{25} V. Beiu, J. Frigo, and K.R. Moore
On the Reliability of Nervous Nets
International Conference on Computational Intelligence for Modeling,
Control and Automation CIMCA’99, Vienna, Austria, February 17-19, 1999

O_{24} S. Draghici and V. Beiu
On Issues Related to VLSI Implementations of Neural Networks
International Conference on Cognitive and Neural Systems CNS’98
Boston, MA, USA, May 27-30, 1998

O_{23} V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins
Digital Implementation of Neural Networks Using Threshold Gates
International Conference Romania and Romanians in Contemporary Science
Sinaia, Romania, May 24-27, 1994
http://citeseerx.ist.psu.edu/viewdoc/citations;jsessionid=E6CF9AE07D31AEDC41844D7E839B9EAB?doi=10.1.1.30.8504

O_{22} D.O. Creteanu and V. Beiu
Systolic Pattern Recognition System
International Conference on Fuzzy Systems and Artificial Intelligence IFSAI’92
Iaşi, Romania, October 28-31, 1992

O_{21} V. Beiu, D.C. Ioan, M. Dumbrava, and O. Robciuc
Physical Fields Determination Using Continuous Boltzmann Machines ***Invited***$_4$
Symposium on Parallel Computing, Bucharest, Romania, December 10-11, 1991

O_{20} V. Beiu: Motion Detection with Neural Networks
International Conference on Industrial and Applied Mathematics ICIAM’91
Washington DC, USA, July 8-12, 1991

O_{19} V. Beiu: Neural Network Solutions for Motion Detection
International Symposium on Applied Informatics, Innsbruck, Austria, February 18-21, 1991

O_{18} A. Florea, V. Beiu, and S. Georgescu
Expert System Development with a Neural Network Simulator
International Conference on AI and Control Systems for Robots AICSR'89
Strbskoe Pleso, Czechoslovakia, November 6-10, 1989

O_{17} V. Beiu: From Systolic Arrays to Neural Networks ***Invited***$_3$
International Symposium on Informatics INFO-IASI'89
Iaşi, Romania, October 19-21, 1989

O_{16} M. Constantinescu and V. Beiu
Theoretical Aspects of Parallel Algorithms for Histogram Modification
International Conference on Computer Systems MICROSYSTEM'89
Carlsbad (Karlovy Vary), Czechoslovakia, September 18-21, 1989

O_{15} V. Beiu and S. Georgescu
Neural Network Models of Vision
IAPR Workshop on Computer Vision, Tokyo, Japan, October 12-14, 1988

O_{14} A. Florea and V. Beiu
Expert Decisions Using Neural Models
Conference on Electronics, Telecommunication, Control and Computers CNETAC'88
Bucharest, Romania, December 7-9, 1988

O_{13} V. Beiu: Hierarchical Memory Enhanced with List Processing Facilities
International Conference on Computer Systems MICROSYSTEM'88
Bratislava, Czechoslovakia, August 30 - September 1, 1988

O_{12} V. Beiu: Parallel Line-Drawing Algorithms
International Conference on Computer Systems MICROSYSTEM'88
Bratislava, Czechoslovakia, August 30 - September 1, 1988

O_{11} V. Beiu. M. Ionescu, E. Paşol, and L. Zuzu
VLSI Implementation of a Statistical Multiplexer
International Symposium Mini and Microcomputers ISMM-MIMI'87
Lugano, Switzerland, June 29 - July 2, 1987

O_{10} V. Beiu, M. Ionescu, E. Paşol, and L. Zuzu
Adaptive Multiplexing Algorithm and Its Possible VLSI Implementation
Mediterranean Electrotechnical Conference MELECON'87, Rome, Italy, March 24-26, 1987

O_9 V. Beiu: Smart Image Memory for Parallel Line Generation
Conference on Electronics, Telecommunication, Control and Computers CNETAC'86
Bucharest, Romania, December 4-6, 1986

O_8 F. Moraru, C. Ispas, S. Constantin, A. Niculescu, and V. Beiu:
Automat Conical Ball Bearing Sorting System
National Conference on Automatic Measurement Systems Using Computer Techniques
Bucharest, Romania, May 22-24, 1986

O_7 V. Beiu: Parallel Adder with Regular Structure
Conference on Electronics, Telecommunication, Control and Computers CNETAC'85
Bucharest, Romania, November 21-23, 1985

O_6 V. Beiu: Self-Testable and Self-Repairable Units – A Must for VLSI Structures
Conference on Electronics, Telecommunication, Control and Computers CNETAC'84
Bucharest, Romania, November 22-24, 1984

O_5 V. Beiu: High Reliability Memory Organization
Conference on Electronics, Telecommunication, Control and Computers CNETAC'83
Bucharest, Romania, November 17-18, 1983

O_4 V. Beiu: Using Microprocessors in Audio Systems
Conference on Electronics, Telecommunication, Control and Computers CNETAC'82
Bucharest, Romania, November 17-19, 1982

O_3 V. Beiu: Memory Structure with Simultaneous Read and Write Capabilities ***Invited$_2$***
Military Academy of Sciences, Bucharest, Romania, November, 1982

O_2 V. Beiu: Method for Storing Digital Information on a Video Recorder
Conference on Electronics, Telecommunication, Control and Computers CNETAC'81
Bucharest, Romania, November, 1981

O_1 V. Beiu: Reliability Enhanced Memory Architecture with Gracefully Degrading Performances ***Invited$_1$***
Jubilee: Ten Years from the Foundation of the National College of Informatics
Bucharest, Romania, May, 1981

TECHNICAL REPORTS 73

Remark: ***28 have appeared only as technical reports, while 45 have also been published (conferences/journals)***
See https://www.osti.gov/search/semantic:Beiu for Los Alamos Unrestricted Reports

TR_{73} V. Dragoi and V. Beiu
Which Coefficients Matter Most — Consecutive k-out-of-n:F Systems Revisited
Tech. Rep. TechRxiv: 23042528/1, 23 May 2023
https://www.techrxiv.org/doi/full/10.36227/techrxiv.23042528.v1

TR_{72} M. Jianu, L. Daus, V. Dragoi, and V. Beiu
Consecutive k-out-of-n:F Systems Have Unbounded Roots
Tech. Rep. arXiv:2208.14173 [cs.DM], 9 August 2022
https://arxiv.org/abs/2208.14173

TR_{71} V. Dragoi, S.R. Cowell, and V. Beiu
Tight Bounds on the Coefficients of Consecutive k-out-of-n:F Systems
Tech. Rep. arXiv:2003.12419 [cs.DM], 27 March 2020
https://arxiv.org/abs/2003.12419

TR_{70} V. Dragoi and V. Beiu
Fast Reliability Ranking of Matchstick Minimal Networks
Tech. Rep. arXiv:1911.01153 [cs.DM], 4 November 2019
https://arxiv.org/abs/1911.01153

TR_{69} M. Nagy, S.R. Cowell, and V. Beiu
Survey of Cubic Fibonacci Identities – When Cuboids Carry Weight
Tech. Rep. arXiv:1902.05944 [math.HO], 15 February 2019
https://arxiv.org/abs/1902.05944

TR_{68} L. Daus, V. Beiu, S.R. Cowell, and P. Poulin
Brick-wall Lattice Paths and Applications
Tech. Rep. arXiv:1804.05277 [math.CO], 14 April 2018
https://arxiv.org/abs/1804.05277

TR_{67} V. Beiu: WTEC-NANO2 (21 pages)
International Study of the Long-term Impacts and Future Opportunities for
Nanoscale Science and Engineering, September 2010

TR$_{66}$ V. Beiu, H.E. Makaruk, D. Morgan, and L. Popa-Simil
ARGOS Advanced RTR (Real Time Radiography) Graphical Object Selection
Los Alamos Unrestricted Report LA-UR-03-2477, April 2003

TR$_{65}$ V. Beiu, H.E. Makaruk, D. Morgan, and L. Popa-Simil
ARGOS – The Problem
Los Alamos Unrestricted Report LA-UR-03-2474, April 2003

TR$_{64}$ V. Beiu: On Automatic Synthesis of Analog/Digital Circuits
Los Alamos Unrestricted Report LA-UR-98-3463, 1998

TR$_{63}$ V. Beiu: Larger Bases and Mixed Analog/Digital Neural Networks
Los Alamos Unrestricted Report LA-UR-98-3462, 1998

TR$_{62}$ V. Beiu, J. Frigo, and K.R. Moore
On the Reliability of Nervous Nets
Los Alamos Unrestricted Report LA-UR-98-3461, 1998

TR$_{61}$ V. Beiu: Neural Inspired Parallel Computations Require Analog Processors
Los Alamos Unrestricted Report LA-UR-98-3325, 1998

TR$_{60}$ V. Beiu and S. Draghici
Designing Constructive Neural Learning Algorithms Based on Information Entropy Bounds
Los Alamos Unrestricted Report LA-UR-98-3168, 1998

TR$_{59}$ V. Beiu: On Kolmogorov's Superposition and Boolean Functions
Los Alamos Unrestricted Report LA-UR-98-2883, 1998

TR$_{58}$ V. Beiu: 2D Neural Hardware vs 3D Biological Ones
Los Alamos Unrestricted Report LA-UR-98-2504, 1998

TR$_{57}$ V. Beiu, S. Draghici, and T. De Pauw
A Constructive Approach to Calculating Lower Entropy Bounds
Los Alamos Unrestricted Report LA-UR-98-2333, 1998

TR$_{56}$ V. Beiu: Implementing Size-Optimal Discrete Neural Networks Requires Analog Circuitry
Los Alamos Unrestricted Report LA-UR-98-1702, 1998

TR$_{55}$ V. Beiu and K.R. Moore
On Analog Implementation of Discrete Neural Networks
Los Alamos Unrestricted Report LA-UR-98-1609, 1998

TR$_{54}$ V. Beiu: How to Build VLSI-Efficient Neural Chips
Los Alamos Unrestricted Report LA-UR-97-4460, 1997

TR$_{53}$ V. Beiu: Implementing Size-Optimal Discrete Neural Networks Requires Analog Circuitry
Los Alamos Unrestricted Report LA-UR-97-4432, 1997

TR$_{52}$ V. Beiu and H.E. Makaruk
On Deeper Nets for Classification Problems
Los Alamos Unrestricted Report LA-UR-97-4413, 1997

TR$_{51}$ V. Beiu and H.E. Makaruk
Deeper and Sparser Nets Are Optimal
Los Alamos Unrestricted Report LA-UR-97-4359, 1997

TR$_{50}$ V. Beiu, S. Draghici, and H.E. Makaruk
On Limited Fan-In Optimal Neural Networks
Los Alamos Unrestricted Report LA-UR-97-4314, 1997

TR$_{49}$ V. Beiu and H.E. Makaruk:
Constructive Entropy Bounds Based on n-Dimensional Complexes
Los Alamos Unrestricted Report LA-UR-97-4251, 1997

TR$_{48}$ V. Beiu and H.E. Makaruk
Small Fan-In Is Beautiful
Los Alamos Unrestricted Report LA-UR-97-3493, 1997

TR$_{47}$ V. Beiu: On the Circuit and VLSI Complexity of Threshold Gate COMPARISON
Los Alamos Unrestricted Report LA-UR-97-3353, 1997

TR$_{46}$ V. Beiu and S. Draghici
On Sparsely Connected Optimal Neural Networks
Los Alamos Unrestricted Report LA-UR-97-2970, 1997

TR$_{45}$ V. Beiu and H.E. Makaruk
Computing Volumes of n-Dimensional Complexes
Los Alamos Unrestricted Report LA-UR-97-2873, 1997

TR$_{44}$ V. Beiu: Entropy, Constructive Neural Learning, and VLSI Efficiency
Los Alamos Unrestricted Report LA-UR-97-2843, 1997

TR$_{43}$ V. Beiu: The Next Generation of Neural Networks Chips
Los Alamos Unrestricted Report LA-UR-97-1917, 1997

TR$_{42}$ V. Beiu: When Reduced Connectivity Neural Networks Are Complexity Optimal?
Los Alamos Unrestricted Report LA-UR-97-1916, 1997

TR$_{41}$ V. Beiu: Digital Integrated Circuit Implementations (of Neural Networks)
Los Alamos Unrestricted Report LA-UR-97-1900, 1997

TR$_{40}$ V. Beiu: Enhanced Lower Entropy Bounds with Application to Constructive Learning
Los Alamos Unrestricted Report LA-UR-97-1877, 1997

TR$_{39}$ S. Draghici, V. Beiu, and I.K. Sethi
A VLSI Optimal Constructive Algorithm for Classification Problems
Los Alamos Unrestricted Report LA-UR-97-1609, 1997

TR$_{38}$ V. Beiu and S. Draghici
On Sparsely Connected Optimal Neural Networks
Los Alamos Unrestricted Report LA-UR-97-1567, 1997

TR$_{37}$ V. Beiu: When Constants Are Important
Los Alamos Unrestricted Report LA-UR-97-1262, 1997

TR$_{36}$ V. Beiu, S. Draghici, and T. De Pauw
A Constructive Approach to Calculating Lower Entropy Bounds
Los Alamos Unrestricted Report LA-UR-97-884, 1997

TR$_{35}$ V. Beiu: Optimization of Circuits Using a Constructive Neural Network Learning Algorithm
Los Alamos Unrestricted Report LA-UR-97-851, 1997

TR$_{34}$ V. Beiu: Enhanced Lower Entropy Bounds with Application to Constructive Learning
Los Alamos Unrestricted Report LA-UR-97-516, 1997

TR$_{33}$ V. Beiu: Reduced Complexity Constructive Learning Algorithm
Los Alamos Unrestricted Report LA-UR-97-515, 1997

TR$_{32}$ S. Draghici and V. Beiu
Entropy Based Comparison of Neural Networks for Classification
Los Alamos Unrestricted Report LA-UR-97-483, 1997

TR$_{31}$ V. Beiu and S. Draghici
Limited Weights Neural Networks: Very Tight Entropy Based Bounds
Los Alamos Unrestricted Report LA-UR-97-294, 1997

TR$_{30}$ V. Beiu: When Constants Are Important
Los Alamos Unrestricted Report LA-UR-97-226, 1997

TR$_{29}$ V. Beiu: Constant Fan-In Discrete Neural Networks Are VLSI-Optimal
Los Alamos Unrestricted Report LA-UR-97-61, 1997

TR$_{28}$ V. Beiu and T. De Pauw
Tight Bounds on the Size of Neural Networks for Classification Problems
Los Alamos Unrestricted Report LA-UR-97-60, 1997

TR$_{27}$ V. Beiu: Optimization of Circuits Using a Constructive Neural Network Learning Algorithm
Los Alamos Unrestricted Report LA-UR-97-59, 1997

TR$_{26}$ V. Beiu: On the Circuit and VLSI Complexity of Threshold Gate COMPARISON
Los Alamos Unrestricted Report LA-UR-96-3591, 1996

TR$_{25}$ V. Beiu: New VLSI Complexity Results for Threshold Gate COMPARISON
Los Alamos Unrestricted Report LA-UR-96-3576, 1996

TR$_{24}$ J.C. Lemm, V. Beiu, and J.G. Taylor
Density Estimation as a Preprocessing Step for Constructive Algorithms
Munster University Technical Report MS-TPI-95-10, 1995

TR$_{23}$ V. Beiu, D.C. Ioan, M. Dumbrava, and O. Robciuc
Physical Fields Determination Using Continuous Boltzmann Machines
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, December 1991

TR$_{22}$ V. Beiu: Motion Detection with Neural Networks
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, September 1991

TR$_{21}$ V. Beiu: Neural Network Solutions for Motion Detection
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, March 1991

TR$_{20}$ V. Beiu: Neural Network Priority Queue
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, October 1990

TR$_{19}$ A. Florea, V. Beiu, and S. Georgescu
Expert System Development with a Neural Network Simulator
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, December 1989

TR$_{18}$ V. Beiu: From Systolic Arrays to Neural Networks
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, November 1989

TR$_{17}$ M. Constantinescu and V. Beiu
Theoretical Aspects of Parallel Algorithms for Histogram Modification
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, October 1989

TR$_{16}$ V. Beiu and A. Florea
Basic Structure of a Program Used to Simulate Processor Networks
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, December 1988

TR$_{15}$ A. Florea and V. Beiu
Expert Decisions Using Neural Models
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, December 1988

TR$_{14}$ V. Beiu: Hierarchical Memory Enhanced with List Processing Facilities
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, October 1988

TR$_{13}$ V. Beiu: Parallel Line-Drawing Algorithms
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, October 1988

TR$_{12}$ V. Ivanov and V. Beiu
Heuristic Simulation of Circuits Using PROLOG
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, February 1988

TR$_{11}$ V. Beiu, M. Ionescu, E. Pasol, and L. Zuzu
VLSI Implementation of a Statistical Multiplexer
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, September 1987

TR$_{10}$ V. Beiu, M. Ionescu, E. Pasol, and L. Zuzu
Adaptive Multiplexing Algorithm and Its Possible VLSI Implementation
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, April 1987

TR$_{9}$ V. Beiu: Smart Image Memory for Parallel Line Generation
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, December 1986

TR$_{8}$ F. Moraru, C. Ispas, S. Constantin, A. Niculescu, and V. Beiu
Automat Conical Ball Bearing Sorting System
Technical Report, Department of Mechanics, University “Politehnica” of Bucharest, Romania, June 1986

TR$_{7}$ V. Beiu: Parallel Adder with Regular Structure
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, December 1985

TR$_{6}$ V. Beiu: Self-Testable and Self-Repairable Units: A Must for VLSI Structures
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, December 1984

TR$_{5}$ V. Beiu: Highly Reliable Memory Organization
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, December 1983

TR$_{4}$ V. Beiu: Memory Structure with Simultaneous Read and Write Capabilities
Technical Report, Military Academy of Sciences, Bucharest, Romania, November 1982

TR$_{3}$ V. Beiu: Using Microprocessors in Audio Systems
Technical Report, Research Institute for Computer Technique, Bucharest, Romania, December 1982

TR$_{2}$ V. Beiu: Method for Recording Digital Information on a Video Recorder
Technical Report, Research Institute for Computer Technique, Bucharest, Romania, December 1981

TR$_{1}$ V. Beiu: Reliability Enhanced Memory with Gracefully Degrading Performances
Technical Report, Research Institute for Computer Technique, Bucharest, Romania, July 1981