

SINTETIC	PUBLICATE	ACCEPTATE
CARTI	2	3
CAPITOLE	8 (7 INVITATE)	5
BREVETE	20	
REVISTE	43 (2 INVITATE)	3 (1 INVITATE)
CONFERINTE	225 (28 INVITATE)	
<b>TOTAL</b>	<b>309 (38 INVITATE, 8 BEST PAPER AWARDS)</b>	
ALTE CONFERINTE RAPOARTE TEHNICE	53 ( 7 INVITATE, 1 BEST PAPER AWARD) 73	

**CARTI** **2**

- V. Beiu and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures  
Book in progress (contract signed with World Scientific)
- V. Beiu: VLSI Complexity of Discrete Neural Networks  
Book in progress (contract signed with Taylor & Francis)
- V. Beiu, R. Andonie, and R. Dogaru: Fundamental Problems of Neural Networks  
Book in progress (contract signed with Technical Printing House)
  
- B<sub>2</sub> V. Beiu and S. Harous (Eds.): Innovations  
IEEE Press, November 2014 (ISBN 9781479972128) 1–132  
<https://doi.org/10.1109/INNOVATIONS.2014.6985768>
- B<sub>1</sub> A. Schmid, S. Goel, W. Wang, V. Beiu, and S. Carrara (Eds.): Nano-Net  
Springer, LNICS, October 2009 (ISBN 9783642024276) 1–286  
<https://doi.org/10.1007/978-3-642-04850-0>
- … V. Beiu: Neural Networks Using Threshold Gates  
A Complexity Analysis of Their Area- and Time-Efficient VLSI Implementations  
PhD dissertation (*summa cum laude*), Katholieke Universiteit Leuven, Leuven, Belgium  
U.D.C. 621.3.04977: 681.3\*C13 (x-27-151779-3), May 1994 1–222

**CAPITOLE (7 INVITED)** **8**

- V. Beiu and W. Ibrahim: On Enabling Redundant Designs for Nano Computations  
In V. Beiu and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures
- V. Beiu, J.M. Quintana, and M.J. Avedillo  
Threshold Logic Design and Implementations: From the Early Days into the Nanoera  
In V. Beiu and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures
- M.H. Sulieman and V. Beiu  
From Single Electron Technology (SET) Full Adders to Optimal Practical SET Adders  
In V. Beiu and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures
- V. Beiu and U. Rückert: Roadmap for Nano Architectures  
In V. Beiu and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures
- J. Nyathi, and V. Beiu: Advanced Techniques for Reducing Power Consumption  
In V. Beiu and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures
  
- Ch<sub>8</sub> V. Beiu, L. Zhang, A. Beg, W. Ibrahim, and M. Tache: Axon-Inspired Communication Systems *Invited*,  
Chapter 15 in J.E. Morris and K. Iniewski (Eds.): Nanoelectronic Device Applications  
Handbook, CRC/Taylor & Francis (UK/USA), 2013 (ISBN 9781466565234) 193–208

Ch <sub>7</sub>	A. Beg, M.H. Sulieman, V. Beiu, and W. Ibrahim: Low-Power Reliable Nano Adders Chapter 6 in J.E. Morris and K. Iniewski (Eds.): Nanoelectronic Device Applications Handbook, CRC/Taylor & Francis (UK/USA), 2013 (ISBN 9781466565234)	<i>Invited<sub>6</sub></i>	67–75
Ch <sub>6</sub>	V. Beiu, W. Ibrahim, and S. Lazarova-Molnar On Device-level Majority von Neumann Multiplexing Chapter 72 in J.R. Rabuñal et al. (Eds.): Encyclopedia of Artificial Intelligence IGI Global, USA (Hershey, PA) and UK (London), 2009 (ISBN 9781599048499) <a href="https://doi.org/10.4018/978-1-59904-849-9.ch072">https://doi.org/10.4018/978-1-59904-849-9.ch072</a>	<i>Invited<sub>5</sub></i>	471–479
Ch <sub>5</sub>	V. Beiu and W. Ibrahim: On Computing Nano-Architectures Using Unreliable Nano-Devices Chapter 12 in S.E. Lyshevski (Ed.): Nano- and Molecular-Electronics Handbook Taylor & Francis (UK/USA), May 2007 (ISBN 9780849385285)	<i>Invited<sub>4</sub></i>	1–49
Ch <sub>4</sub>	V. Beiu: Entropy, Constructive Neural Learning, and VLSI Efficiency In R. Andonie, and D. Grosu (Eds.): Neural Priorities in Data Transmission and EDA Tempus SJEPE 8180-94, "Transilvania" Univ. of Braşov, Braşov, Romania, 1998	<i>Invited<sub>3</sub></i>	38–74
Ch <sub>3</sub>	V. Beiu: Constant Fan-in Discrete Neural Networks Are VLSI-Optimal Chapter 12 in S.W. Ellacott, J.C. Mason, and I.J. Anderson (Eds.) Mathematics of Neural Networks Models, Algorithms and Applications Kluwer Academic, Boston, MA, USA, 1997 (ISBN 9781461377948) <a href="https://doi.org/10.1007/978-1-4615-6099-9_12">https://doi.org/10.1007/978-1-4615-6099-9_12</a>		89–94
Ch <sub>2</sub>	V. Beiu: Digital Integrated Circuit Implementations (of Neural Networks) Chapter E1.4 in E. Fiesler, and R. Beale (Eds.): Handbook of Neural Computations Institute of Physics, New York, NY, USA, 1996 (ISBN 9780750303125)	<i>Invited<sub>2</sub></i>	E1.4.1–34
Ch <sub>1</sub>	V. Beiu: Optimal VLSI Implementations of Neural Networks Chapter 18 in J.G. Taylor (Ed.): Neural Networks and Their Applications John Wiley & Sons, Chichester, UK, 1996 (ISBN 9780471962823)	<i>Invited<sub>1</sub></i>	255–276

**BREVETE (SINGUR AUTOR LA TOATE)**

**20**

	– V. Beiu: Procedure Enabling Statistical Meaningful Evaluation of Any Physical Feature or Figure-of-Merit of a Digital or Analog Circuit UAEU Intellectual Property Disclosure, Jul. 16, 2014 & Feb. 11, 2015 (Rouse Ref. U0018-00167)		
P <sub>20</sub>	V. Beiu: Low-Power Differential Conductance-Based Logic Gate and Method of Operation Thereof (Washington, DC, USA, June 17, 2003) US40319573 <a href="https://patentscope.wipo.int/search/en/detail.jsf?docId=US40319573">https://patentscope.wipo.int/search/en/detail.jsf?docId=US40319573</a>		1–18
P <sub>18,19</sub>	V. Beiu: Microprocessor and a Digital Signal Processor Including Adder and Multiplier Circuits Employing Logic Gates Having Discrete and Weighted Inputs (February 4, 2003) US39973941 <a href="https://patentscope.wipo.int/search/en/detail.jsf?docId=US39973941">https://patentscope.wipo.int/search/en/detail.jsf?docId=US39973941</a> US39287083 <a href="https://patentscope.wipo.int/search/en/detail.jsf?docId=US39287083">https://patentscope.wipo.int/search/en/detail.jsf?docId=US39287083</a>		1–14
P <sub>17</sub>	V. Beiu: Adder Circuits Employing Logic Gates Having Discrete Weighted Inputs and a Method of Operation Therewith (Washington, DC, USA, December 31, 2002) US39287082 <a href="https://patentscope.wipo.int/search/en/detail.jsf?docId=US39287082">https://patentscope.wipo.int/search/en/detail.jsf?docId=US39287082</a>		1–13
P <sub>13-16</sub>	V. Beiu: Adder Having Reduced Number of Internal Layers and Method of Operation Thereof (Washington, DC, USA, August 20, 2002) AU180986431 <a href="https://patentscope.wipo.int/search/en/detail.jsf?docId=AU180986431">https://patentscope.wipo.int/search/en/detail.jsf?docId=AU180986431</a> TW 493139 <a href="https://twpat1.tipo.gov.tw/tipotwoc/tipotwekm?!!FR_493139">https://twpat1.tipo.gov.tw/tipotwoc/tipotwekm?!!FR_493139</a> US39682800 <a href="https://patentscope.wipo.int/search/en/detail.jsf?docId=US39682800">https://patentscope.wipo.int/search/en/detail.jsf?docId=US39682800</a> WO2001023992 <a href="https://patentscope.wipo.int/search/en/detail.jsf?docId=WO2001023992">https://patentscope.wipo.int/search/en/detail.jsf?docId=WO2001023992</a>		1–11

- P<sub>9-12</sub> V. Beiu: Noise Tolerant Conductance-Based Logic Gate and Methods of Operation and Manufacturing Thereof (Washington, DC, USA, August 6, 2002) 1–16  
 AU180951667 <https://patentscope.wipo.int/search/en/detail.jsf?docId=AU180951667>  
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- P<sub>8</sub> V. Beiu: Logic Gate Having Reduced Power Dissipation and Method of Operation Thereof (Washington, DC, USA, July 10, 2001) 1–19  
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- P<sub>2-7</sub> V. Beiu: Adder and Multiplier Circuits Employing Logic Gates Having Discrete, Weighted Inputs and Methods of Performing Combinatorial Operations Therewith (March 20, 2001) 1–14  
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 US39353335 <https://patentscope.wipo.int/search/en/detail.jsf?docId=US39353335>  
 US39287081 <https://patentscope.wipo.int/search/en/detail.jsf?docId=US39287081>  
 WO2000017802 <https://patentscope.wipo.int/search/en/detail.jsf?docId=WO2000017802>
- P<sub>1</sub> V. Beiu: LSI Unit for Mutual Exclusion  
 Dispozitiv de excludere mutuala a unor sarcini referitoare la controlul asupra unor resurse 1–12  
 RO 84763, April 26, 1984 <https://patents.google.com/patent/RO84763B1/en>

**REVISTE (3 INVITATE)**

**43**

- ... V. Beiu et al.: The Curse of Constant Failure Rates, Inputs and Averaging – A Comprehensive Review In planning  
 ... V. Beiu et al.: Brain-inspired Computing Revisited – Why Energy Consumption Is So Elusive In progress  
 ... V. Beiu et al.: Revisiting Schmitt Trigger Tolerance to Variations In progress  
 ... V. Beiu, R.-M. Beiu, and V. Dragoi: The Trustworthy Wings of the Mysterious Butterflies To be submitted
- J<sub>46</sub> S.R. Cowell, S. Hoara, and V. Beiu: Approximating Hammocks' Reliability with Beta Distributions  
 Intl. J. Comp. Comm. & Ctrl. (IF ~ 2.635, SJR ~ 0.499) Accepted
- J<sub>45</sub> V. Beiu: Brain Inspired Nano Architectures *Invited,*  
 Intl. J. Comp. Comm. & Ctrl. (IF ~ 2.635, SJR ~ 0.499) Accepted
- J<sub>44</sub> M. Tache and V. Beiu: When Non-Gaussian Distributions Have to Be Considered  
 Theory and Applications of Mathematics & Computer Science Accepted
- J<sub>43</sub> V. Dragoi and V. Beiu  
 Which Coefficients Matter Most – Consecutive- $k$ -out-of- $n$ :F Systems Revisited  
 IEEE Trans. Reliab., vol. 73, no. 3, Sep. 2024 (IF ~ 5.9, SJR ~ 1.296) 1633–1646  
<https://doi.org/10.1109/TR.2024.3353908>
- J<sub>42</sub> M. Nagy, S.R. Cowell, and V. Beiu  
 On the Construction of 3D Fibonacci Spirals  
 Mathematics, vol. 12, no. 2, Jan. 2024 (IF ~ 2.4, SJR ~ 0.446) art. 201 (1–19)  
<https://doi.org/10.3390/math12020201>
- J<sub>41</sub> M. Jianu, L. Daus, V. Dragoi, and V. Beiu  
 The Roots of the Reliability Polynomials of Circular Consecutive- $k$ -out-of- $n$ :F Systems  
 Mathematics, vol. 11, no. 20, Oct. 2023 (IF ~ 2.4, SJR ~ 0.446) art. 4252 (1–12)  
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- J<sub>40</sub> M. Jianu, L. Daus, V. Dragoi, and V. Beiu  
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Fast Reliability Ranking of Matchstick Minimal Networks **Highly cited**  
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- J<sub>38</sub> M. Nagy, S.R. Cowell, and V. Beiu  
Survey of Cubic Fibonacci Identities – When Cuboids Carry Weight  
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<https://doi.org/10.15837/ijccc.2022.2.4616>
- J<sub>37</sub> V. Beiu, L. Daus, M. Jianu, A. Mihai, and I. Mihai  
On a Surface Associated with Pascal’s Triangle  
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<https://doi.org/10.3390/sym14020411>
- J<sub>36</sub> V. Dragoi, S.R. Cowell, and V. Beiu  
Four Input Sorter Good, Larger Ones Not So Good  
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- J<sub>35</sub> V. Dragoi and V. Beiu  
Studying the Binary Erasure Polarization Subchannels Using Network Reliability  
IEEE Comm. Lett., vol. 24, no. 1, Jan. 2020 (IF = 3.436, SJR = 0.929) 62–66  
<https://doi.org/10.1109/LCOMM.2019.2947910>
- J<sub>34</sub> V. Dragoi, S.R. Cowell, V. Beiu, S. Hoara, and P. Gaspar  
How Reliable Are Compositions of Series and Parallel Networks  
Compared with Hammocks?  
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- J<sub>33</sub> M. Tache, W. Ibrahim, F. Kharbash, and V. Beiu  
Reliability and Performance of Optimised Schmitt Trigger Gates  
IET Journal of Engineering, vol. 2018, no. 8, Aug. 2018 735–744  
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- J<sub>31</sub> S.R. Cowell, V. Beiu, L. Daus, and P. Poulin  
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- J<sub>30</sub> R.-M. Beiu, V. Beiu, and V.-F. Duma  
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 Ultra-Low Voltage/Power/Energy Gates  
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<https://doi.org/10.1166/jolpe.2014.1305>
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<http://www.oldcitypublishing.com/journals/ijuc-home/ijuc-issue-contents/ijuc-volume-8-number-4-2012/ijuc-8-4-p-325-332/>
- J<sub>24</sub> W. Ibrahim, V. Beiu, and A. Beg  
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- V. Beiu: Why Neural Energy/Power Is So Elusive In progress
- M. Tache et al.: From Trust (Reliable) to Dust (Silicon Chips) – Bridging the Network-Circuit Divide In progress

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 Nanostructured Fiber Optics as Highly Sensitive Mechanical Sensors  
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 Dubai, UAE, September 26-28, 2005  
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Iasi, Romania, October 28-31, 1992
- O<sub>21</sub> V. Beiu, D.C. Ioan, M. Dumbrava, and O. Robciuc *Invited<sub>4</sub>*  
Physical Fields Determination Using Continuous Boltzmann Machines  
Symposium on Parallel Computing, Bucharest, Romania, December 10-11, 1991
- O<sub>20</sub> V. Beiu: Motion Detection with Neural Networks  
International Conference on Industrial and Applied Mathematics ICIAM'91  
Washington DC, USA, July 8-12, 1991

- O<sub>19</sub> V. Beiu: Neural Network Solutions for Motion Detection  
International Symposium on Applied Informatics, Innsbruck, Austria, February 18-21, 1991
- O<sub>18</sub> A. Florea, V. Beiu, and S. Georgescu  
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- O<sub>6</sub> V. Beiu: Self-Testable and Self-Repairable Units – A Must for VLSI Structures  
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- O<sub>3</sub> V. Beiu: Memory Structure with Simultaneous Read and Write Capabilities *Invited<sub>2</sub>*  
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- O<sub>2</sub> V. Beiu: Method for Storing Digital Information on a Video Recorder  
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- O<sub>1</sub> V. Beiu: Reliability Enhanced Memory Architecture with Gracefully Degrading Performances *Invited<sub>1</sub>*  
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