FIŞA DE VERIFICARE

A ÎNDEPLINIRII STANDARDELOR MINIMALE

pentru ocuparea posturilor didactice şi de cercetare (adaptată după metodologia proprie UAV)

I. DATE DESPRE CANDIDAT

NUME	Beiu
PRENUME	Valeriu
CNP	
Postul pentru care candideaza	Profesor universitar
Disciplinele	Fundamente ale reţelelor neuronale biologice Probleme computaţionale ale reţelelor neuronale artificiale Modelarea şi optimizarea deciziilor Sisteme informatice în comerţ şi turism
Poziţia în statul de funcţii	10
Departamentul	Departamentul de Matematică-Informatică
Facultatea	Facultatea de Ştiinţe Exacte
Gradul didactic actual	Profesor (plata cu ora)
Poziţia în Statul de funcţii:	8, 10, 21 (Ştiinţe Exacte) şi 15 (Inginerie)
Discipline	Fundamente ale reţelelor neuronale biologice Probleme computaţionale ale reţelelor neuronale artificiale Proiect de cercetare în circuite inteligente
Departamentul	Departamentul de Matematică-Informatică Departamentul de Automatică, Inginerie Industrială, Textile şi Transporturi
Facultatea	Facultatea de Ştiinţe Exacte Facultatea de Inginerie
Universitatea	Universitatea „Aurel Vlaicu” din Arad

II. DATE PRIVIND ÎNDEPLINIREA CONDIŢIILOR DE CONCURS

1. Studii universitare de licenţă şi masterat

Nr. crt.	Instituţia de învăţământ superior	Domeniul	Perioada	Titlul acordat
1	Institutul Politehnic din Bucureşti (Universitatea Politehnica din Bucureşti) Facultatea de Automatică (Facultatea de Automatică şi Calculatoare) Secţia de Automatizări şi Calculatoare (Secţia de Calculatoare)	Profilul Electric	1975 - 1980	Diplomă de Inginer Specializarea Automatizări şi Calculatoare

2. Studii universitare de doctorat

Nr. crt.	Instituţia organizatoare de doctorat	Domeniul	Perioada	Titlul acordat
1	Katholieke Universiteit Leuven (Leuven, Belgium) Facultatea de Ştiinte Aplicate	Ştiinte Aplicate	1991 - 1994	Doctor în Ştiinte Aplicate

Detalii despre domeniul ştiintelor aplicate ("domein Toegepaste Wetenschappen") la KULeuven
http://www.kuleuven.be/onderzoek/onderzoeksdatabank/project/T000.htm

3. Studii şi burse postdoctorale

Nr. crt.	Instituţia organizatoare	Domeniul	Perioada	Obs.
1	King's College London (Londra, Anglia) Center for Neural Networks Department of Mathematics	Neural Networks Programmable Neural Arrays	1994 - 1996	EU Human Capital and Mobility (HCM) Individual Postdoctoral Fellow
2	Los Alamos National Laboratory (Los Alamos, NM, SUA) Space and Atmospheric Sciences (Space Electronics and Signal Processing)	Neural Networks Programmable Neural Arrays	1996 - 1998	Director's Postdoctoral Fellow

4. Grade didactice/profesionale

Nr. crt.	Instituţia organizatoare	Domeniul	Perioada	Titlul/Funcţia
1	Institutul Politehnic din Bucureşti Facultatea de Automatică Secţia de Automatizări şi Calculatoare	Automatizări şi Calculatoare	1983 - 1990	Asistent
2	Universitatea Politehnica din Bucureşti Facultatea de Automatică şi Calculatoare Secţia de Calculatoare	Calculatoare	1990 - 2001	Şef de lucrări
3	Washington State University School of Electrical Engineering and Computer Science Department of Computer Engineering	Computer Engineering	2001 - 2005	Conferenţiar
4	United Arab Emirates University College of Information Technology Department of Computer System Design	Computer System Design	2005 - 2008	Conferenţiar
5	United Arab Emirates University College of Information Technology Department of Computer System Design	Computer System Design	2008 - 2015	Profesor
6	Universitatea „Aurel Vlaicu” din Arad Facultatea de Ştiinţe Exacte Domeniul Informatică (Informatică Aplicată în Ştiinţe, Tehnologie şi Economie) Facultatea de Inginerie Domeniul Ingineria Sistemelor (Automatică şi Informatică Aplicată)	Informatică Aplicată în Ştiinţe, Tehnologie şi Economie Automatică şi Informatică Aplicată	2015 - ……	Profesor (plata cu ora)

III. DATE PRIVIND ÎNDEPLINIREA STANDARDELOR SPECIFICE

4. *Profesor universitar*

a.	Deţine titlul ştiinţific de doctor	Atestat Nr. 37182 din 14.XI.1995 (copie legalizată inclusa la F)	Îndeplinit
b.	În cazul în care nu a deţinut un post didactic universitar pe o perioada de minim 2 ani, certificarea competentelor pedagogice prin diploma de master didactic/certificat de absolvire a modulului psiho-pedagogic II sau documente echivalente	Am deţinut un post didactic universitar începand din 1983 (peste 30 de ani)	Îndeplinit

c. Fişa de verificare a standardelor minimale naţionale conform fişei de verificare a comisiei de informatica (OMECTS Nr. 890bis/27.XII.2012, Anexa nr. 2, pp. 4-5) | Conform tabelului de mai jos şi a dovezilor justificative (incluse în continuare) | Îndeplinit

Indicatori de performanţă **Performance criterion**	**Punctaj minim** **Minimum values**	**Punctaj realizat** **Self-evaluation**	**Îndeplinit / Neîndeplinit**
Perspectiva B **Producţia ştiinţifică** ***Scientific output***			
A + B + C	56	292.72	Îndeplinit
A	24	176.66	Îndeplinit
B	16	88.00	Îndeplinit
Perspectiva C **Impactul rezultatelor** ***Scientific impact***			
A + B + C + D	120	2674.45	Îndeplinit
A+B	40	1996.53	Îndeplinit
Perspectiva D **Performanţa academică** ***Academic performance***	60	679.25	Îndeplinit

TOTAL	**236**	**3650.42**	Îndeplinit

Auto-evaluarea a fost realizată în perioada decembrie-ianuarie 2017 folosind
https://informatica-universitaria.ro/
http://informatica-universitaria.ro/ppages/16/
http://informatica-universitaria.ro/php/index.html
http://www.core.edu.au/conference-portal
http://portal.core.edu.au/conf-ranks/

Data completării
13.01.2017

Candidat,

Verificat:

Preşedinte comisie: .....

Membrii comisie: .....

.....

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.....

.....

VALERIU BEIU

B. PRODUCTIA STIITIFICA

OVERVIEW	NR. & CLASS / SCORE		MIN REQUIRED
JOURNALS	9 x A	72.00	–
	6 x B	24.00	–
	3 x C	2.06	–
CONFERENCES	16 x A	104.66	–
	18 x B	64.00	–
	17 x C	30.00	–
	TOTAL A	176.66 >	24
	TOTAL B	88 >	16
	TOTAL C	32.06	–
TOTAL (A+B+C)		296.72 >	56

JOURNALS 98.06

B_6 V. Beiu, and L. Dauş: Reliability Bounds for Two Dimensional Consecutive Systems *Invited*$_2$
Nano Communication Networks, vol. 6, no. 3, Sept. 2015 (IF announced, SJR ~ 0.618)
Special Issue on Biological Information and Communication Technology 145–152
4 4 / max(1, n-2) = 4 / max(1, 2-2) = 4 / 1 = 4

B_5 L. Dauş, and V. Beiu: Lower and Upper Reliability Bounds for Consecutive-*k*-out-of-*n*:F Systems
IEEE Transactions on Reliability, vol. 64, no. 3, Sept. 2015 (IF = 2.287, SJR = 1.930) 1128–1135
4 4 / max(1, n-2) = 4 / max(1, 2-2) = 4 / 1 = 4

C_3 M. Tache, V. Beiu, W. Ibrahim, F. Kharbash, and M. Alioto
Enhancing the Static Noise Margins by Sizing Length for *Invited*$_1$
Ultra-Low Voltage/Power/Energy Gates
Journal of Low Power Electronics, vol. 10, no. 1, Mar. 2014 (SJR = 0.186) 137–148
0.66 2 / max(1, n-2) = 2 / max(1, 5-2) = 2 / 3 = 0.66

C_2 G. Wendin, D. Vuillaume, M. Calame, S. Yitzchaik, C. Gamrat, G. Cuniberti, and V. Beiu
SYMONE Project: SYnaptic MOlecular NEtworks for Bio-inspired Information Processing
Journal of Unconventional Computing, vol. 8, no. 4, Nov. 2012 (IF = 0.431, SJR = 0.205) 325–332
0.40 2 / max(1, n-2) = 2 / max(1, 7-2) = 2 / 5 = 0.40

B_4 W. Ibrahim, V. Beiu, and A. Beg: Optimum Reliability Sizing for CMOS Gates
IEEE Transactions on Reliability, vol. 61, no. 3, Sept. 2012 (IF = 2.293, SJR = 1.516) 675–686
4 4 / max(1, n-2) = 4 / max(1, 3-2) = 4 / 1 = 4

A_9 W. Ibrahim, V. Beiu, and A. Beg
GREDA: A Fast and More Accurate CMOS Gates Reliability EDA Tool
IEEE Transactions on Computer-Aided Design of Integrated Circuits & Systems
vol. 31, no. 4, Apr. 2012 (IF = 1.093, SJR = 0.790) 509–521
8 8 / max(1, n-2) = 8 / max(1, 3-2) = 8 / 1 = 8

B_3 W. Ibrahim, and V. Beiu
Using Bayesian Networks to Accurately Calculate the Reliability of CMOS Gates
IEEE Transactions on Reliability, vol. 60, no. 3, Sept. 2011 (IF = 1.285, SJR = 1.337) 538–549
4 4 / max(1, n-2) = 4 / max(1, 2-2) = 4 / 1 = 4

	A_8	V. Beiu, and W. Ibrahim: Devices and Input Vectors Are Shaping von Neumann Multiplexing	
		IEEE Transactions on Nanotechnology, vol. 10, no. 3, May 2011 (IF = 2.292, SJR = 1.271)	606–616
8		8 / max(1, n-2) = 8 / max(1, 2-2) = 8 / 1 = 8	
	C_1	V. Beiu, B.A.M. Madappuram, P.M. Kelly, and L.J. McDaid	
		On Two-layer Brain-inspired Hierarchical Topologies — A Rent's Rule Approach	
		Transactions on High-Performance Embedded Architecture and Compilers (HiPEAC) IV	
		P. Stenström (Ed.), Springer LNCS 6769, Jan. 2011	311–333
1		2 / max(1, n-2) = 2 / max(1, 4-2) = 2 / 2 = 1	
	A_7	W. Ibrahim, and V. Beiu: Threshold Voltage Variations Make Full Adders Reliabilities Similar	
		IEEE Transactions on Nanotechnology, vol. 9, no. 6, Nov. 2010 (IF = 1.864, SJR = 1.203)	664–667
8		8 / max(1, n-2) = 8 / max(1, 2-2) = 8 / 1 = 8	
	A_6	W. Ibrahim, V. Beiu, and M.H. Sulieman: On the Reliability of Majority Gates Full Adders	
		IEEE Transactions on Nanotechnology, vol. 7, no. 1, Jan. 2008 (IF = 2.154, SJR = 1.387)	56–67
8		8 / max(1, n-2) = 8 / max(1, 3-2) = 8 / 1 = 8	
	A_5	M.H. Sulieman, and V. Beiu: On Single Electron Technology Full Adders	
		IEEE Transactions on Nanotechnology, vol. 4, no. 6, Nov. 2005 (IF = 2.112, SJR = 2.455)	669–680
8		8 / max(1, n-2) = 8 / max(1, 2-2) = 8 / 1 = 8	
	A_4	S. Roy, and V. Beiu	
		Majority Multiplexing — Economical Redundant Fault-Tolerant Design for Nano Architectures	
		IEEE Transactions on Nanotechnology, vol. 4, no. 4, Jul. 2005 (IF = 2.112, SJR = 2.455)	441–451
8		8 / max(1, n-2) = 8 / max(1, 2-2) = 8 / 1 = 8	
	A_3	V. Beiu, J.M. Quintana, and M.J. Avedillo	
		VLSI Implementations of Threshold Gates — A Comprehensive Survey	
		IEEE Transactions on Neural Networks, vol. 14, no. 5, Sept. 2003 (IF = 1.666, SJR = 1.727)	
		Special Issue on Hardware Implementations of Neural Networks	1217–1243
8		8 / max(1, n-2) = 8 / max(1, 3-2) = 8 / 1 = 8	
	B_2	V. Beiu, S. Draghici, and T. De Pauw	
		A Constructive Approach to Calculating Lower Entropy Bounds	
		Neural Processing Letters, vol. 9, no. 1, Feb. 1999 (IF = 0.405, SJR = 1.162)	1–12
4		4 / max(1, n-2) = 4 / max(1, 3-2) = 4 / 1 = 4	
	B_1	V. Beiu, and H.E. Makaruk: Deeper Sparsely Nets Can Be Optimal	
		Neural Processing Letters, vol. 8, no. 3, Dec. 1998 (IF = 0.286, SJR later)	201–210
4		4 / max(1, n-2) = 4 / max(1, 2-2) = 4 / 1 = 4	
	A_2	V. Beiu: On the Circuit and VLSI Complexity of Threshold Gate COMPARISON	
		Neurocomputing, vol. 19, no. 1, Apr. 1998 (IF = 0.453, SJR later)	77–98
8		8 / max(1, n-2) = 8 / max(1, 1-2) = 8 / 1 = 8	
	A_1	V. Beiu, and J.G. Taylor: On the Circuit Complexity of Sigmoid Feedforward Neural Networks	
		Neural Networks, vol. 9, no. 7, Oct. 1996 (IF = 1.325, SJR later)	1155–1171
8		8 / max(1, n-2) = 8 / max(1, 2-2) = 8 / 1 = 8	

JOURNALS	**9 x A**	**72.00**	**>**	**24**
	6 x B	**24.00**	**>**	**16**
	3 x C	**2.06**		
	TOTAL	**98.06**	>	**56**

	C_{17}	P. Santagati, and V. Beiu: A Mathematical Model for the Analysis of the Johnson-Nyquist Noise on the Reliability of Nano-Communications International Conference on Bio-Inspired Models of Network, Information, and Computing Systems BIONETICS'12, Lugano, Switzerland, December 10-12, 2012 In G.A. Di Caro, and G. Theraulaz (eds.), Springer, LNICST vol. 134, July 2014	49–62
2		2 / max(1, n-2) = 2 / max(1, 2-2) = 2 / 1 = 2	
	A_{16}	J.J. Wade, L.J. McDaid, J. Harkin, V. Crunelli, J.A.S. Kelso, and V. Beiu Exploring Retrograde Signaling via Astrocytes as a Mechanism for Self Repair IEEE International Joint Conference on Neural Networks IJCNN'11 San Jose, CA, USA, July 31 - August 5, 2011	3149–3155
2		8 / max(1, n-2) = 8 / max(1, 6-2) = 8 / 4 = 2	
	C_{16}	V. Beiu, B.A.M. Madappuram, P.M. Kelly, and L.J. McDaid On Two-layer Hierarchical Networks: How Does the Brain Do This? International ICST Conference on Nano-Networks Nano-Net'09 Luzern, Switzerland, October 18-20, 2009 In A. Schmid et al. (eds.), Springer, LNICST vol. 20, October 2009	*Invited*$_{24}$ 231–241
1		2 / max(1, n-2) = 2 / max(1, 4-2) = 2 / 2 = 1	
	C_{15}	P.M. Kelly, F. Tuffy, V. Beiu, and L.J. McDaid: Reduced Interconnects in Neural Networks Using a Time Multiplexed Architecture Based on Quantum Devices International ICST Conference on Nano-Networks Nano-Net'09 Luzern, Switzerland, October 18-20, 2009 In A. Schmid et al. (eds.), Springer, LNICST vol. 20, October 2009	*Invited*$_{23}$ 242–250
1		2 / max(1, n-2) = 2 / max(1, 4-2) = 2 / 2 = 1	
	C_{14}	V. Beiu, W. Ibrahim, and R.Z. Makki: On Wires Holding a Handful of Electrons International ICST Conference on Nano-Networks Nano-Net'09 Luzern, Switzerland, October 18-20, 2009 In A. Schmid et al. (eds.), Springer, LNICST vol. 20, October 2009	*Invited*$_{22}$ 259–269
2		2 / max(1, n-2) = 2 / max(1, 3-2) = 2 / 1 = 2	
	C_{13}	W. Ibrahim, and V. Beiu A Bayesian-based EDA Tool for Nano-Circuits Reliability Calculations International ICST Conference on Nano-Networks Nano-Net'09 Luzern, Switzerland, October 18-20, 2009 In A. Schmid et al. (eds.), Springer, LNICST vol. 20, October 2009	*Invited*$_{21}$ 276–284
2		2 / max(1, n-2) = 2 / max(1, 2-2) = 2 / 1 = 2	
	A_{15}	V. Beiu, and W. Ibrahim: On CMOS Circuit Reliability from the MOSFETs and the Input Vectors IEEE/IFIP International Conference on Dependable Systems and Networks DSN'09 [workshop] Estoril, Lisbon, Portugal, June 29 - July 2, 2009 http://www.laas.fr/WDSN09/WDSN09_files/Texts/WDSN09-2-2-Beiu.pdf	
4		[8 / max(1, n-2)] / 2 = [8 / max(1, 2-2)] / 2 = [8 / 1] / 2 = 4	
	A_{14}	V. Beiu, and W. Ibrahim: Does the Brain Really Outperform Rent's Rule? IEEE International Symposium on Circuits and Systems ISCAS'08 Seattle, WA, USA, May 18-21, 2008	640–643
8		8 / max(1, n-2) = 8 / max(1, 2-2) = 8 / 1 = 8	

	C_{12}	S. Lazarova-Molnar, V. Beiu, and W. Ibrahim Reliability – The Fourth Optimization Pillar of Nanoelectronics IEEE International Conference on Signal Processing and Communications ICSPC'07 Dubai, UAE, November 24-27, 2007 73–76
2		2 / max(1, n-2) = 2 / max(1, 3-2) = 2 / 1 = 2
	C_{11}	W. Ibrahim, and V. Beiu: Why Nano-DSP Will Be Fan-in Constrained IEEE International Conference on Signal Processing and Communications ICSPC'07 Dubai, UAE, November 24-27, 2007 317–320
2		2 / max(1, n-2) = 2 / max(1, 2-2) = 2 / 1 = 2
	A_{13}	W. Ibrahim, and V. Beiu: Long Live Small Fan-in Majority Gates – Their Reign Looks Like Coming! IEEE International Conference on Application-specific Systems Architectures and Processors ASAP'07, Montreal, Canada, July 8-11, 2007 278–283
8		8 / max(1, n-2) = 8 / max(1, 2-2) = 8 / 1 = 8
	B_{18}	V. Beiu, W. Ibrahim, and S. Lazarova-Molnar What von Neumann Did Not Say About Multiplexing: Beyond Gates Failures – The Gory Details International Work-Conference on Artificial Neural Networks IWANN'07 San Sebastián, Spain, June 19-22, 2007, Springer LNCS 4507 487–496
4		4 / max(1, n-2) = 4 / max(1, 3-2) = 4 / 1 = 4
	C_{10}	M.H. Sulieman, and V. Beiu: Multiplexing Schemes for Single Electron Technologies IEEE International Conference on Computer Systems and Applications AICCSA'06 Sharjah, UAE, March 8-11, 2006 424–428
2		2 / max(1, n-2) = 2 / max(1, 2-2) = 2 / 1 = 2
	C_9	V. Beiu, J. Nyathi, S. Aunet, and M.H. Sulieman: Femto Joule Switching for Nano Electronics IEEE International Conference on Computer Systems and Applications AICCSA'06 Sharjah, UAE, March 8-11, 2006 415–423
1		2 / max(1, n-2) = 2 / max(1, 4-2) = 2 / 2 = 1
	A_{12}	V. Beiu, and A. Zawadzki On Kolmogorov's Superpositions: Novel Gates and Circuits for Nanoelectronics? IEEE International Joint Conference on Neural Networks IJCNN'05 Montreal, Canada, July 31 - August 4, 2005 651–656
8		8 / max(1, n-2) = 8 / max(1, 2-2) = 8 / 1 = 8
	A_{11}	S. Aunet, and V. Beiu: Ultra Low Power Fault Tolerant Neural Inspired CMOS Logic IEEE International Joint Conference on Neural Networks IJCNN'05 Montreal, Canada, July 31 - August 4, 2005 2843–2848
8		8 / max(1, n-2) = 8 / max(1, 2-2) = 8 / 1 = 8
	A_{10}	V. Beiu, S. Aunet, J. Nyathi, R. Rydberg III, and A. Djupdal On the Advantages of Serial Architectures for Low-Power Reliable Computations IEEE International Conference on Application-specific Systems, Architectures and Processors ASAP'05, Samos, Greece, July 23-25, 2005 276–281
2.66		8 / max(1, n-2) = 8 / max(1, 5-2) = 8 / 3 = 2.66
	B_{17}	V. Beiu, A. Djupdal, and S. Aunet Ultra Low-Power Neural Inspired Addition – When Serial Might Outperform Parallel Architectures International Work-Conference on Artificial Neural Networks IWANN'05 Barcelona, Spain, June 8-10, 2005, Springer LNCS 3512 486–493
4		4 / max(1, n-2) = 4 / max(1, 3-2) = 4 / 1 = 4

	B_{16}	V. Beiu, A. Zawadzki, R. Andonie, and S. Aunet Using Kolmogorov Inspired Gates for Low Power Nanoelectronics International Work-Conference on Artificial Neural Networks IWANN'05 Barcelona, Spain, June 8-10, 2005, Springer LNCS 3512	438–445
2		4 / max(1, n-2) = 4 / max(1, 4-2) = 4 / 2 = 2	
	A_9	V. Beiu: A Novel Highly Reliable Low-Power Nano Architecture When von Neumann Augments Kolmogorov	*Invited*$_{16}$
		IEEE International Conference on Application-specific Systems, Architectures and Processors ASAP'04, Galveston, TX, USA, September 27-29, 2004	167–177
8		8 / max(1, n-2) = 8 / max(1, 1-2) = 8 / 1 = 8	
	A_8	J. Nyathi, V. Beiu, S. Tatapudi, and D.J. Betwoski A Charge Recycling Differential Noise-Immune Perceptron IEEE International Joint Conference on Neural Networks IJCNN'04 Budapest, Hungary, July 25-29, 2004	1995–2000
4		8 / max(1, n-2) = 8 / max(1, 4-2) = 8 / 2 = 4	
	A_7	M.H. Sulieman, and V. Beiu Characterization of a 16-bit Threshold Logic Single Electron Technology Adder IEEE International Symposium on Circuits and Systems ISCAS'04 Vancouver, Canada, May 23-26, 2004	681–684
8		8 / max(1, n-2) = 8 / max(1, 2-2) = 8 / 1 = 8	
	C_8	P.-S. Wu, and V. Beiu On Accurate Piecewise Linear ROM-less Direct Digital Frequency Synthesizers IEEE International Conference on Neural Networks and Signal Processing ICNNSP'03 Nanjing, China, December 14-17, 2003	1595–1599
2		2 / max(1, n-2) = 2 / max(1, 2-2) = 2 / 1 = 2	
	C_7	M.H. Sulieman, and V. Beiu: Optimal Practical Adders Using Perceptrons IEEE International Conference on Neural Networks and Signal Processing ICNNSP'03 Nanjing, China, December 14-17, 2003	345–348
2		2 / max(1, n-2) = 2 / max(1, 2-2) = 2 / 1 = 2	
	C_6	D.J. Betowski, and V. Beiu Considerations for Phase Accumulator Design for Direct Digital Frequency Synthesizers IEEE International Conference on Neural Networks and Signal Processing ICNNSP'03 Nanjing, China, December 14-17, 2003	176–179
2		2 / max(1, n-2) = 2 / max(1, 2-2) = 2 / 1 = 2	
	A_6	R. Andonie, L. Sasu, and V. Beiu: Fuzzy ARTMAP with Relevance Factor IEEE International Joint Conference on Neural Networks IJCNN'03 Portland, OR, USA, July 20-24, 2003	1975–1980
8		8 / max(1, n-2) = 8 / max(1, 3-2) = 8 / 1 = 8	
	A_5	V. Beiu: A Survey of Perceptron Circuit Complexity Results IEEE International Joint Conference on Neural Networks IJCNN'03 Portland, OR, USA, July 20-24, 2003	989–994
8		8 / max(1, n-2) = 8 / max(1, 1-2) = 8 / 1 = 8	

	B_{15}	V. Beiu: Constructive Threshold Logic Addition – A Synopsis of the Last Decade International Conference on Artificial Neural Networks ICANN'03 Istanbul, Turkey, June 26-29, 2003, Springer LNCS 2714 745–752
4		4 / max(1, n-2) = 4 / max(1, 1-2) = 4 / 1 = 4
	B_{14}	V. Beiu, J.M. Quintana, and M.J. Avedillo: Review of Capacitive Threshold Gate Implementations International Conference on Artificial Neural Networks ICANN'03 Istanbul, Turkey, June 26-29, 2003, Springer LNCS 2714 737–744
4		4 / max(1, n-2) = 4 / max(1, 3-2) = 4 / 1 = 4
	B_{13}	S. Tatapudi, and V. Beiu: Split-Precharge Differential Noise-Immune Threshold Logic Gate International Work-Conference on Artificial Neural Networks IWANN'03 Menorca, Spain, June 3-6, 2003, Springer LNCS 2687 49–56
4		4 / max(1, n-2) = 4 / max(1, 2-2) = 4 / 1 = 4
	A_4	V. Beiu: On Higher Order Noise Immune Perceptrons IEEE International Joint Conference on Neural Networks IJCNN'01 Washington, DC, USA, July 14-19, 2001, vol. 1 246–251
8		8 / max(1, n-2) = 8 / max(1, 1-2) = 8 / 1 = 8
	B_{12}	V. Beiu: Neural Addition and Fibonacci Numbers International Work-Conference on Artificial Neural Networks IWANN'99 Alicante, Spain, June 2-4, 1999, Springer LNCS 1607 198–207
4		4 / max(1, n-2) = 4 / max(1, 1-2) = 4 / 1 = 4
	B_{11}	V. Beiu: Larger Bases and Mixed Analog/Digital Neural Networks International Conference on Artificial Neural Networks in Engineering ANNIE'98 St. Louis, MI, USA, November 1-4, 1998. In C.H. Dagli et al. (Eds.), ASME Press 63–70
4		4 / max(1, n-2) = 4 / max(1, 1-2) = 4 / 1 = 4
	B_{10}	V. Beiu, and K.R. Moore: On Analog Implementation of Discrete Neural Networks International Workshop on Fuzzy Logic and Intelligent Technologies FLINS'98 Antwerp, Belgium, September 14-16, 1998, World Scientific 258–265
4		4 / max(1, n-2) = 4 / max(1, 2-2) = 4 / 1 = 4
	B_9	V. Beiu: Implementing Size-Optimal Discrete Neural Networks Requires Analog Circuitry European Signal Processing Conference EuSiPCo'98 Island of Rhodes, Greece, September 8-11, 1998, vol. 3 1325–1328
4		4 / max(1, n-2) = 4 / max(1, 1-2) = 4 / 1 = 4
	A_3	V. Beiu, and H.E. Makaruk: Small Fan-In Is Beautiful IEEE International Joint Conference on Neural Networks IJCNN'98 Anchorage, AL, USA, May 4-9, 1998, vol. 2 1321–1326
8		8 / max(1, n-2) = 8 / max(1, 2-2) = 8 / 1 = 8
	B_8	S. Draghici, V. Beiu, and I.K. Sethi: A VLSI Optimal Constructive Algorithm International Conference on Artificial Neural Networks in Engineering ANNIE'97 St. Louis, MI, USA, November 9-12, 1997, ASME Press 145–151
4		4 / max(1, n-2) = 4 / max(1, 3-2) = 4 / 1 = 4
	C_5	V. Beiu: Optimization of Circuits Using a Constructive Neural Network Learning Algorithm International Conference on Engineering Applications of Neural Networks EANN'97 Stockholm, Sweden, June 16-18, 1997, Åbo Akademis 291–194
2		2 / max(1, n-2) = 2 / max(1, 1-2) = 2 / 1 = 2

	B_7	V. Beiu, and T. De Pauw: Tight Bounds on the Size of Neural Networks for Classification Problems International Work-Conference on Artificial Neural Networks IWANN'97 Lanzarote, Canary Islands, Spain, June 4-6, 1997, Springer LNCS 1240	743–752
4		4 / max(1, n-2) = 4 / max(1, 2-2) = 4 / 1 = 4	
	C_4	J.C. Lemm, V. Beiu, and J.G. Taylor Density Estimation as a Preprocessing Step for Constructive Algorithms International Symposium on Neural Network ISNN'95 Nijmegen, The Netherlands, September 14-15, 1995, Springer	213–216
2		2 / max(1, n-2) = 2 / max(1, 3-2) = 2 / 1 = 2	
	B_6	V. Beiu, and J.G. Taylor: Optimal Mapping of Neural Networks onto FPGAs International Workshop on Artificial Neural Networks IWANN'95 Málaga, Spain, June 7-9, 1995, Springer LNCS 930	822–829
4		4 / max(1, n-2) = 4 / max(1, 2-2) = 4 / 1 = 4	
	C_3	V. Beiu, and J.G. Taylor: VLSI Optimal Learning Algorithm International Conference on Artificial Neural Networks and Genetic Algorithms ICANNGA'95 Alès, France, April 19-21, 1995, Springer	61–64
2		2 / max(1, n-2) = 2 / max(1, 2-2) = 2 / 1 = 2	
	A_2	V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins Placing Feedforward Neural Networks Among Several Circuit Complexity Classes World Conference on Neural Networks WCNN'94 San Diego, CA, USA, June 4-9, 1994, Lawrence Erlbaum & INNS Press, vol. 2	584–589
4		8 / max(1, n-2) = 8 / max(1, 4-2) = 8 / 2 = 4	
	B_5	V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins On the Circuit Complexity of Feedforward Neural Networks International Conference on Artificial Neural Networks ICANN'94 Sorrento, Italy, May 26-29, 1994, Springer	521–524
2		4 / max(1, n-2) = 4 / max(1, 4-2) = 4 / 2 = 2	
	B_4	V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins VLSI Complexity Reduction by Piece-Wise Approximation of the Sigmoid Function European Symposium on Artificial Neural Networks ESANN'94 Brussels, Belgium, April 20-22, 1994, D facto	*Invited*$_5$ 181–186
2		4 / max(1, n-2) = 4 / max(1, 4-2) = 4 / 2 = 2	
	C_2	D.O. Creteanu, V. Beiu, J.A. Peperstraete, and R. Lauwereins Systolic Pattern Recognition Based on a Neural Network Algorithm International Conference on Artificial Neural Networks and Genetic Algorithms ICANNGA'93 Innsbruck, Austria, April 13-16, 1993, Springer	137–144
1		2 / max(1, n-2) = 2 / max(1, 4-2) = 2 / 2 = 1	
	B_3	V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins Efficient Decomposition of Comparison and Its Applications European Symposium on Artificial Neural Networks ESANN'93 Brussels, Belgium, April 7-9, 1993, D facto	45–50
2		4 / max(1, n-2) = 4 / max(1, 4-2) = 4 / 2 = 2	

	A_1	V. Beiu, J.A. Peperstraete, and R. Lauwereins: Simpler Neural Networks by Fan-in Reduction IEEE International Joint Conference on Neural Networks IJCNN'92 Beijing, China, November 3-6, 1992, vol. 3 204–209
8		8 / max(1, n-2) = 8 / max(1, 3-2) = 8 / 1 = 8
	B_2	V. Beiu, J.A. Peperstraete, and R. Lauwereins Using Threshold Gates to Implement Sigmoid Nonlinearities International Conference on Artificial Neural Networks ICANN'92 Brighton, UK, September 4-7, 1992, Elsevier 1447–1450
4		4 / max(1, n-2) = 4 / max(1, 3-2) = 4 / 1 = 4
	B_1	V. Beiu: Neural Network for Digital Image Enhancement International Conference on Artificial Neural Networks ICANN'91 Espoo, Finland, June 24-28, 1991, Elsevier, vol. 2 1071–1074
4		4 / max(1, n-2) = 4 / max(1, 1-2) = 4 / 1 = 4
	C_1	V. Beiu: VLSI Arrays Implementing Parallel Line-Drawing Algorithms International Workshop on Parallel Processing by Cellular Automata PARCELLA'88 Berlin, Germany, October 17-21, 1988, Springer LNCS vol. 342 241–247
2		2 / max(1, n-2) = 2 / max(1, 1-2) = 2 / 1 = 2

	Journals			Conferences			
	A	B	C	A	B	C	
1	8	4	1	8	4	2	1
2	8	4	0.40	4	4	1	2
3	8	4	0.66	8	2	2	3
4	8	4		8	2	2	4
5	8	4		8	2	2	5
6	8	4		8	4	2	6
7	8			8	4	2	7
8	8			4	4	2	8
9	8			8	4	1	9
10				2.66	4	2	10
11				8	4	2	11
12				8	4	2	12
13				8	4	2	13
14				8	4	2	14
15				4	4	1	15
16				2	2	1	16
17					4	2	17
18					4		18
	72	24	2.06	104.66	64	30	
		Journals	98.06		Conferences	198.66	

A	B	C
176.66	88	32.06

TOTAL 296.72

PhD	PhD dissertation					V. Beiu	Neural Networks Using Threshold Gates -- A Complexity Analysis of Their Area- and Time-Efficient VLSI Implementations	Katholieke Universiteit Leuven	Leuven, Belgium	May 1994	1 - 222
	IWANN-97	B	4	4		S. Draghici and I.K. Sethi	On the possibilities of the limited precision weights neural networks in classification problems	International Work-Conference on Artificial and Natural Neural Networks (LNCS 1240)	Lanzarote, Spain	4-6 Jun. 1997	753 - 762
	Chapter	D	1	0		P. Moerland and E. Fiesler	Neural Network Adaptations to Hardware Implementations	Handbook of Neural Computations	IoP & Oxford Univ.Press	Jan. 1997	E1.2 1 - 13
	scitech	D	1	0		H.E. Makaruk	Computations of Entropy Bounds: Multidimensional Geometric Methods	Los Alamos National Laboratory LA-UR--97-4413	DOE, USA	Feb. 1998	1 - 10
	Journal	B	4	4		S. Draghici	Neural Networks in Analog Hardware -- Design and Implementation Issues	**International Journal of Neural Systems**	Vol. 10, No. 1	Feb. 2000	19 - 42
	PhD	D	1	0		J. Yang	In-The-Loop Training of a VLSI Implementation of a Smart Sensor with Low Resolution Programmable Digital Weights	University of Windsor	Windsor, ON, Canada	May 2000	1 - 217
	Book	B	4	4		M.N. Cristea et al.	Neural and Fuzzy Logic Control of Drives and Power Systems	Elsevier	Oxford, UK	Jul. 2002	1 - 399
	Journal	A	8	8		S. Draghici	On the Capabilities of Neural Networks Using Limited Precision	**Neural Networks**	Vol. 15, No. 3	Apr. 2002	395 - 414
	ieee	D	1	0		A. Dinu and M.	A Digital Neural Network FPGA Direct Hardware Implementation	IEEE International Symposium on Industrial Eelectronics	Vigo, Spain	4-7 Jun. 2007	2307 - 2312
	Journal	A	8	8		A. Ahmadi et al.	An Associative Memory-based Learning Model with an Efficient Hardware Implementation in FPGA	**Expert Systems with Applications**	Vol. 38, No. 4	Apr. 2011	3499 - 3513
32.00			32	28	28.00						

B01	Book					A. Schmid, S. Goel, W. Wang, V. Beiu, and S. Carrara	Nano-Net	ISBN 978-3-642-02427-6	Springer, LNICS	Oct. 2009	1 - 286
	Journal	C	2	0		N. Aliakbarinodehi et al.	Electrochemical Nanostructured Biosensors: Carbon Nanotubes versus Conductive and Semi-conductive Nanoparticles	**Chemical Papers**	Vol. 69, No. 1	Jan. 2015	134 - 142
	Journal	B	4	4		O. Vazquez-Mena et al.	Resistless nanofabrication by stencil lithography: A review	**Microelectronic Engineering**	Vol. 132	25 Jan. 2015	236 - 254
	ieee	D	1	0		N. Farsad et al.	A Comprehensive Survey of Recent Advancements in Molecular Communication	**IEEE Communications Surveys & Tutorials**	Vol. 18, No. 3	Sept. 2016	1887 - 1919
	Journal	B	4	4		J. Hammond et al.	Electrochemical biosensors and nanobiosensors	**Essays in Biochemistry**	Vol. 60, No. 1	Jun. 2016	69 - 80
	ISCAS-10	C	2	0		V. Erokhin	Organic Memristors: Basic Principles	IEEE International Symposium on Circuits and Systems	Paris, France	30 May - 2 Jun. 2010	5 - 8
	ieee	D	1	0		V. Erokhin and M.P. Fontana	Organic Memristive Device and Its Application for the Information Processing	IEEE International Conference on Electronics, Circuits and Systems	Athens, Greece	12-15 Dec. 2010	926 - 929
	Journal	B	4	4		V. Erokhin et al.	Bio-inspired Adaptive Networks Based on Organic Memristors	**Nano Communication Networks**	Vol. 1, No. 2	Jun. 2010	108 - 117
	Journal	A	8	8		C. Boero et al.	Targeting of Multiple Metabolites in Neural Cells Monitored by Using Protein-Based Carbon Nanotubes	**Sensors and Actuators B: Chemical**	Vol. 157, No. 1	Sept. 2011	216 - 224
	PhD	D	1	0		M.A. Kotlarchyk	Optical Measurement of Micromechanics and Structure in a 3D Fibrin Extracellular Matrix (UMI 3482434)	University of California Irvine	Irvine, CA, USA	2011	1 - 154

	Journal	**A**	**8**	**8**		Y. Nazarenko et al.	Potential for Inhalation Exposure to Engineered Nanoparticles from Nanotechnology-Based Cosmetic Powders	**Environmental Health Perspectives**	Vol. 120, No. 6	Jun. 2012	885 - 892
11.67			**35**	**28**	**9.33**						
B05	**Book**					**V. Beiu, and U. Rückert**	**Emerging Brain-Inspired Nano-Architectures**	**Book accepted and in progress**	**World Scientific**	**Contract signed in 2005**	
	Journal	**A**	**8**	**8**		C. Gao and D. Hammerstrom	Cortical Models onto CMOL and CMOS – Architectures and Performance/Price	**IEEE Transactions on Circuit and Systems I**	Vol. 54, No. 11	Nov. 2007	2502 - 2515
	PhD	**D**	**1**	**0**		C. Gao	Hardware Architectures and Implementations for Associative Memories -- The Building Blocks of Hierarchically Distributed Memories (UMI 3346835)	Portland State University	Portland, OR, USA	2008	1 - 209
	WCCI-08	**A**	**8**	**8**		C. Gao et al.	CMOS / CMOL Architectures for Spiking Cortical Column	IEEE World Congress on Computational Intelligence (WCCI-08)	Hong Kong	1-6 Jun. 2008	2441 - 2448
	Journal	**A**	**8**	**8**		M.S. Zaveri and D. Hammerstrom	CMOL/CMOS Implementations of Bayesian Polytree Inference: Digital and Mixed-Signal Architectures and Performance/Price	**IEEE Transactions on Nanotechnology**	Vol. 9, No. 2	Mar. 2010	194 - 211
25.00			**25**	**24**	**24.00**						
C013	**CompEuro-87**					**V. Beiu, and C. Constantinescu**	**Fault-Tolerant Systolic Arrays for Antialiasing**	**Annual European Computer Conference**	**Hamburg, Germany**	**11-15 May 1987**	**720 - 723**
	Journal	**D**	**1**	**0**		C. Constantinescu	Effect of Transient Faults on Gracefully Degrading Processor Arrays	**Microprocessing and Microprogramming**	Vol. 26, No. 1	Mar. 1989	23 - 30
1.00			**1**	**0**	**0.00**						
C019	**CompEuro-89**					**V. Beiu, and S. Georgescu**	**Consideration of Vision Based on Associative Neural Networks**	**IEEE Annual European Computer Conference**	**Hamburg, Germany**	**8-12 May 1989**	**121 - 124**
	IAPR-92	**B**	**4**	**4**		E. Sicard et al.	An Integrated Approach to Real-time Pattern Recognition	International Conference on Pattern Recognition	Vol. IV	30 Aug - 3 Sept, 1992	177 - 180
4.00			**4**	**4**	**4.00**						
C025	**ICANN'91**					**V. Beiu**	**Neural Network for Digital Image Enhancement**	**International Conference on Artificial Neural Networks**	**Espoo, Finland**	**24-28 Jun. 1991**	**1071 - 1074**
	acm	**D**	**1**	**0**		P.G. Kim et al.	Handwritten Hangul Recognition by Stroke Representation	ACM International Conference on Young Computer Scientists	Beijing, China	15-17 Jul. 1993	833 - 836
1.00			**1**	**0**	**0.00**						
C028	**CompEuro-92**					**V. Beiu, D.C. Ioan, and M.C. Dumbrava**	**Continuous Boltzmann Machines: Theoretical Aspects and Applications**	**IEEE European Computer Conference**	**Hague, Netherlands**	**4-8 May 1992**	**193 - 198**
	PhD	**D**	**1**	**0**		E.M. Farguell	A new approach to Decimation in High Order Boltzmann Machines	Department of Electrical Engineering, Ramon Llull University	Barcelona, Spain	20 Jan. 2011	1 - 238
1.00			**1**	**0**	**0.00**						

C029	**ICANN-92**					**V. Beiu, J.A. Peperstraete, and R. Lauwereins**	**Using Threshold Gates to Implement Sigmoid Nonlinearities**	**International Conference on Artificial Neural Networks**	**Brighton, UK**	**4-7 Sept. 1992**	**1447 - 1450**
	ICNN-95	**B**	**4**	**4**		A. Basaglia et al.	Behavior-driven Minimal Implementation of Digital ANNs	IEEE International Conference on Neural Networks	Perth, Australia	27 Nov. - 1 Dec. 1995	1644 - 1649
4.00			**4**	**4**	**4.00**						
C030	**NeuroNimes-92**					**V. Beiu, J.A. Peperstraete, and R. Lauwereins**	**Algorithms for Fan-in Reduction**	**International Conference on Neural Networks and Their Applications**	**Nîmes, France**	**2-6 Nov. 1992**	**589 - 600**
	ICNN-95	**B**	**4**	**4**		D. Elizondao et al.	Non-ontogenic Sparse Neural Networks	IEEE International Conference on Neural Networks	Perth, Australia	27 Nov. - 1 Dec. 1995	290 - 295
	Journal	**B**	**4**	**4**		D. Elizondo and E. Fiesler	A Survey of Partially Connected Neural Networks	**International Journal of Neural Systems**	Vol. 8, No. 5 & 6	Oct./Dec. 1997	535 – 558
8.00			**8**	**8**	**8.00**						
C031	**IJCNN-92**					**V. Beiu, J.A. Peperstraete, and R. Lauwereins**	**Simpler Neural Networks by Fan-in Reduction**	**IEEE International Joint Conference on Neural Networks**	**Beijing, China**	**3-6 Nov. 1992**	**204 - 209**
	Journal	**A**	**8**	**8**		S. Draghici	On the Capabilities of Neural Networks Using Limited Precision Weights	**Neural Networks**	Vol. 15, No. 3	Apr. 2002	395 - 414
8.00			**8**	**8**	**8.00**						
C034	**ESANN-93**					**V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins**	**Efficient Decomposition of Comparison and Its Applications**	**European Symposium on Artificial Neural Networks ESANN'93**	**Brussels, Belgium**	**7-9 Apr. 1993**	**45 - 50**
	PhD	**D**	**1**	**0**		Y. Sun	Computer Architectures Using Nanotechnology (UMI 3493764)	Lehigh University	Bethlehem, PA, USA	Jan. 2012	1 - 104
0.50			**1**	**0**	**0.00**						
C036	**CSCS-9**					**V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins**	**Overview of Some Efficient Threshold Gate Decomposition Algorithms**	**International Conference on Control System and Computer Science**	**Bucharest, Romania**	**25-28 May 1993**	**458 - 469**
	PhD	**D**	**1**	**0**		V. Annampedu	Nanotechnology Architectures for Pattern Matching (UMI 3270646)	Lehigh University	Bethlehem, PA, USA	2007	1 - 179
	PhD	**D**	**1**	**0**		Y. Sun	Computer Architectures Using Nanotechnology (UMI 3493764)	Lehigh University	Bethlehem, PA, USA	Jan. 2012	1 - 104
	Journal	**A**	**8**	**8**		V. Annampedu and M.D. Wagh	Decomposition of Threshold Functions into Bounded Fan-in Threshold Functions	**Information and Computation**	Vol. 227	Jun. 2013	84 - 101
5.00			**10**	**8**	**4.00**						

C037	**ICYCS-93**					**V. Beiu, J.A. Peperstraete, and R. Lauwereins**	**Enhanced Threshold Gate Fan-In Reduction Algorithms**	**International Conference for Young Computer Scientists**	**Beijing, China**	**15-17 Jul. 1993**	**3.39 - 3.42**
	PhD	**D**	**1**	**0**		V. Annampedu	Nanotechnology Architectures for Pattern Matching (UMI 3270646)	Lehigh University	Bethlehem, PA, USA	2007	1 - 179
	Journal	**A**	**8**	**8**		V. Annampedu and M.D. Wagh	Decomposition of Threshold Functions into Bounded Fan-in Threshold Functions	**Information and Computation**	Vol. 227	Jun. 2013	84 - 101
	arXiv	**D**	**1**	**0**		F. Shi et al.	An Enhanced Multiway Sorting Network Based on n-Sorters	Computer Research Repository	Online	Jul. 2014	1 - 13
	ieee	**D**	**1**	**0**		F. Shi et al.	An Enhanced Multiway Sorting Network Based on n-Sorters	IEEE Global Conference on Signal and Information Processing	Atlanta, GA, USA	3-5 Dec. 2014	60 - 64
11.00			**11**	**8**	**8.00**						

C039	**ESANN-94**					**V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins**	**VLSI Complexity Reduction by Piece-Wise Approximation of the Sigmoid Function**	**European Symposium on Artificial Neural Networks**	**Brussels, Belgium**	**20-22 Apr. 1994**	**181 - 186**
	CiteSeerX	**D**	**1**	**0**		C.A. Galicia and R.R.L. Ascencio	A CPLD Implementation of an Artificial Neural Network for Instrumentation Applications	International Workshop on Design of Mixed-mode Integrated Circuits and Applications	Guanajuato, Mexico	27-29 Jul. 1998	96 - 99
	CiteSeerX	**D**	**1**	**0**		M.G. Hernández et al.	An Artificial Neural Network on a Complex Programmable Logic Device as a Virtual Sensor	International Symposium on Robotics and Automation	Saltillo, Mexico	12-14 Dec. 1998	1 - 5
	CiteSeerX	**D**	**1**	**0**		M.G. Hernández et al.	The Study of a Prototype of an Artificial Neural Network on a Field Programmable Gate Array as a Function Approximator	International Workshop on Design of Mixed-mode Integrated Circuits and Applications	Guanajuato, Mexico	27-29 Jul. 1998	1 - 4
	ieee	**D**	**1**	**0**		M.G. Hernández et al.	The Study of a Prototype of an Artificial Neural Network on a FPGA as a Function Approximator	IEEE International Workshop on Design of Mixed-Mode Integrated Circuits and Applications	Puerto Vallarta, Mexico	26-28 Jul. 1999	126 - 129
	ieee	**D**	**1**	**0**		M.A.A. Leon et al	An Artificial Neural Network on an FPGA as a Virtual Sensor	IEEE International Workshop on Design of Mixed-Mode Integrated Circuits and Applications	Puerto Vallarta, Mexico	26-28 Jul. 1999	114 - 117
	ieee	**D**	**1**	**0**		S. Marra et al.	Tanh-like Activation Function Implementation for High-performance Digital Neural Systems	IEEE International Conference on PhD Research in Microelectronics and Electronics	Otranto, Italy	12-15 Jun. 2006	237 - 240
	PhD	**D**	**1**	**0**		R. Eickhoff	Fehlertolerante Neuronale Netze zur Approximation von Funktionen	University of Paderborn	Paderborn, Germany	11 Jul. 2007	1 - 260
	ICANN-07	**B**	**4**	**4**		R. Eickhoff et al.	Impact of Shrinking Technologies on the Activation Function of Neurons	International Conference on Artificial Neural Networks (LNCS 4668)	Porto, Portugal	9-13 Sept. 2007	501 - 510
	IJCNN-07	**A**	**8**	**8**		S. Marra et al.	High Speed, Programmable Implementation of a Tanh-like Activation Function and Its Derivative for Digital Neural Networks	IEEE International Joint Conferece on Neural Networks	Orlando, FL, USA	12-17 Aug. 2007	506 - 511
	ISCA-11	**A**	**8**	**8**		R.F. Astudillo and J.P. da Silva Neto	Propagation of Uncertainty through Multilayer Perceptrons for Robust Automatic Speech Recognition	Annual Conference of the International Speech Communication Association	Florence, Italy	28-31 Aug. 2011	461 - 464
	InterSpeech-15	**A**	**8**	**8**		A.H. Abdelaziz et	Uncertainty Propagation Through Deep Neural Networks	Annual Conference of the International Speech Communication	Dresden,	6-10 Sept.	3561 - 3565
	InterSpeech-15	**A**	**8**	**8**		C. Huemmer et	Uncertainty Decoding for DNN-HMM Hybrid Systems Based on	Annual Conference of the International Speech Communication	Dresden,	6-10 Sept.	3556 - 3560
21.50			**43**	**36**	**18.00**						

C040	**SPRANN-94**					**V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins**	**Area-Time Performances of Some Neural Computations**	**International Symposium on Signal Processing, Robotics, and Artificial Neural Networks**	**Lille, France**	**25-27 Apr. 1994**	**664 - 668**
	IWANN-97	**B**	**4**	**4**		S. Draghici and	On the possibilities of the limited precision weights neural	International Work-Conference on Artificial and Natural Neural	Lanzarote, Spain	4-6 Jun. 1997	753 - 762
2.00			**4**	**4**	**2.00**						
C041	**ICANN-94**					**V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins**	**On the Circuit Complexity of Feedforward Neural Networks**	**International Conference on Artificial Neural Networks**	**Sorrento, Italy**	**26-29 May 1994**	**521 - 524**
	Journal	**A**	**8**	**8**		S. Draghici	On the Capabilities of Neural Networks Using Limited Precision	**Neural Networks**	Vol. 15, No. 3	Apr. 2002	395 - 414
4.00			**8**	**8**	**4.00**						
C042	**WCNN-94**					**V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins**	**Placing Feedforward Neural Networks Among Several Circuit Complexity Classes**	**World Conference on Neural Networks**	**San Diego, CA, USA**	**4-9 Jun. 1994**	**584 - 589**
	Journal	**A**	**8**	**8**		P.W.C. Prasad and A. Beg	Investigating Data Preprocessing Methods for Circuit Complexity Models	**Expert Systems with Applications**	Vol. 36, No. 1	Jan. 2009	519 - 526
4.00			**8**	**8**	**4.00**						
C045	**ICANNGA-95**					**V. Beiu, and J.G. Taylor**	**VLSI Optimal Learning Algorithm**	**International Conference on Artificial Neural Networks and Genetic Algorithms**	**Alès, France**	**19-21 Apr. 1995**	**61 - 64**
	IWANN-97	**B**	**4**	**4**		S. Draghici and I.K. Sethi	On the possibilities of the limited precision weights neural networks in classification problems	International Work-Conference on Artificial and Natural Neural Networks (LNCS 1240)	Lanzarote, Spain	4-6 Jun. 1997	753 - 762
	IlliGAL	**D**	**1**	**0**		D.E. Goldberg	Genetic Algorithms: A Bibliography	Univ. of Illinois at Urbana-Champaign, Illinois Genetic Algorithms Laboratory (IlliGAL), Tech. Rep. 2000037	Urbana-Champaign, IL, USA	Jan. 2000	1 - 380
5.00			**5**	**4**	**4.00**						
C046	**CSCS-10**					**V. Beiu, and J.G. Taylor**	**Area-Efficient Constructive Learning Algorithm**	**International Conference on Control System and Computer Science**	**Bucharest, Romania**	**24-26 May 1995**	**293 - 310**
	CiteSeerX	**D**	**1**	**0**		G. Thimm and E. Fiesler	A Neural Networks Construction Method based on Boolean Logic	Short version in IEEE International Conference on Tools with Artificial Intelligence	Toulouse, France	16-19 Nov. 1996	458 - 459
	IWANN-97	**B**	**4**	**4**		S. Draghici and I.K. Sethi	On the possibilities of the limited precision weights neural networks in classification problems	International Work-Conference on Artificial and Natural Neural Networks (LNCS 1240)	Lanzarote, Spain	4-6 Jun. 1997	753 - 762
5.00			**5**	**4**	**4.00**						
C047	**IWANN-95**					**V. Beiu, and J.G. Taylor**	**Optimal Mapping of Neural Networks onto FPGAs**	**International Workshop on Artificial Neural Networks**	**Málaga, Spain**	**7-9 Jun. 1995**	**822 - 829**
	Chapter	**D**	**1**	**0**		R. Andonie	The "Psychological" Limits of Neural Computation	In M. Kárný, K. Warwick, and V. Kůrková (Eds.): "Dealing with Complexity: A Neural Networks Approach"	Springer	Dec. 1997	252 - 263
	ieee	**D**	**1**	**0**		A. Dinu et al.	Virtual Prototyping of a Digital Neural Current Controller	IEEE International Workshop on Rapid System Prototyping	Leuven, Belgium	3-5 Jun. 1998	176 - 181

	IWANN-99	B	4	4		J.M. Moreno et al.	The Role of Dynamic Reconfiguration for Implementing Artificial Neural Networks Models in Programmable Hardware	International Work-conference on Artificial Neural Networks (LNCS 1607)	Alicante, Spain	2-4 Jun. 1999	85 - 94
	Book	B	4	4		M.N. Cristea et al.	Neural and Fuzzy Logic Control of Drives and Power Systems	Elsevier	Oxford, UK	Jul. 2002	1 - 399
	CiteSeerX	D	1	0		N.H.F. Beebe	A Bibliography of Papers in Lecture Notes in Computer Science (2005), Part 1 of 4	Department of Mathematics, University of Utah	Salt Lake, UT, USA	29 Jul. 2005	1 - 219
11.00			**11**	**8**	**8.00**						

C048	**SNN-95**					**J.C. Lemm, V. Beiu, and J.G. Taylor**	**Density Estimation as a Preprocessing Step for Constructive Algorithms**	**Annual Symposium on Neural Network**	**Nijmegen, The Netherlands**	**14-15 Sept. 1995**	**213 - 216**
	acm	D	1	0		J.C. Lemm	Prior Information and Generalized Questions	ACM -- MIT, AI Lab Memo No. 1598	Cambridge, MA	Dec. 1996	1 - 93
	arXiv	D	1	0		J.C. Lemm	Bayesian Field Theory	arXiv:physics/9912005 v3		7 Mar. 2000	1 - 200
	Book	A	8	8		J.C. Lemm	Bayesian Field Theory: Nonparametric Approaches to Density Estimation	John Hopkins University Press	Baltimore, MA, USA	Jun. 2003	1 - 432
10.00			**10**	**8**	**8.00**						

C049	**MicroNeuro-96**					**V. Beiu, and J.G. Taylor**	**Direct Synthesis of Neural Networks**	**IEEE International Conference on Microelectronics for Neural Networks**	**Lausanne, Switzerland**	**12-14 Feb. 1996**	**257 - 264**
	Chapter	D	1	0		P. Moerland and E. Fiesler	Neural Network Adaptations to Hardware Implementations	Handbook of Neural Computations	IoP & Oxford Univ.Press	Jan. 1997	E1.2 1 - 13
	Journal	B	4	4		L. Nemes et al.	Implementation of arbitrary Boolean functions on a CNN universal machine	**International Journal of Circuit Theory and Applications**	Vol. 26, No. 6	Nov./Dec. 1998	593 - 610
	Journal	B	4	4		D.M. Hanna et al.	Using a System-on-a-Chip Implantable Device to Filter Circulating Infected Cells in Blood or Lymph	**IEEE Transactions on Nanobioscience**	Vol. 2, No. 1	Mar. 2003	6 - 13
	PhD	D	1	0		J. Sima	Neuronové Síte Jako Modely Analogových Výpoctu	Academy of the Czech Republic	Prague, Czech Republic	Apr. 2006	1 - 46
10.00			**10**	**8**	**8.00**						

C050	**AT-96**					**V. Beiu**	**VLSI Complexity of Threshold Gate COMPARISON**	**International Symposium on Neuro-Fuzzy Systems**	**Lausanne, Switzerland**	**29-31 Aug. 1996**	**161 - 170**
	Journal	D	1	0		J.B. da Fonseca	From a New Way to Show the Universality of a Two-Layer Perceptron to a New Approach to Digital Design	**WSEAS Transactions on Systems and Controls**	Vol. 5, No. 4	Apr. 2006	892 - 897
1.00			**1**	**0**	**0.00**						

C051	**SBRN-96**					**V. Beiu**	**New VLSI Complexity Results for Threshold Gate COMPARISON**	**Brazilian Symposium on Neural Networks**	**Recife, Brazil**	**12-14 Nov. 1996**	**251 - 258**
	IWANN-03	B	4	4		E. Burattini et al.	NSP: A Neuro-symbolic Processor	International Work-Conference on Artificial and Natural Neural Networks (LNCS 2687)	Maá, Menorca, Spain	3-6 Jun. 2003	9 - 16
4.00			**4**	**4**	**4.00**						

C052	**WIRN-Vietri-97**					**S. Draghici, and V. Beiu**	**Entropy Based Comparison of Neural Networks for Classification**	**Italian Workshop on Neural Nets**	**Vietri sul Mare, Salerno, Italy**	**22-24 May 1997**	**124 - 132**
	springer	D	1	0		S. Draghici	On the Complexity of VLSI-friendly Neural Networks for Classification Problems	Biennial Conference of the Canadian Society for Computational Studies of Intelligence (LNCS 1418)	Vancouver, Canada	18-20 Jun. 1998	285 - 297
	IJCNN-98	A	8	8		S. Draghici	Using Information Entropy Bounds to Design VLSI Friendly	IEEE International Joint Conference on Neural Networks	Ankorage, AK,	4-9 May 1998	547 - 552

	PhD	**D**	**1**	**0**		J. Yang	In-The-Loop Training of a VLSI Implementation of a Smart Sensor with Low Resolution Programmable Digital Weights	University of Windsor	Windsor, ON, Canada	May 2000	1 - 217
	PhD	**D**	**1**	**0**		J.M.F. dos Santos	Data Classification with Neural Networks and Entropic Criteria	University of Porto	Porto, Portugal	Jan. 2007	1 - 212
11.00			**11**	**8**	**8.00**						
C053	**CSCS-11**					**V. Beiu**	**When Constants Are Important**	**International Conference on Control System and Computer Science**	**Bucharest, Romania**	**28-31 May 1997**	**106 - 111**
	ieee	**D**	**1**	**0**		L.K. Scheffer	Design Tools for Artificial Nervous Systems	ACM/EDAC/IEEE Design Automation Conference	San Francisco, CA, USA	3-7 Jun. 2012	717 - 722
1.00			**1**	**0**	**0.00**						
C054	**IWANN-97**					**V. Beiu, and T. De Pauw**	**Tight Bounds on the Size of Neural Networks for Classification Problems**	**International Work-Conference on Artificial Neural Networks**	**Lanzarote, Canary Islands, Spain**	**4-6 Jun. 1997**	**743 - 752**
	IWANN-97	**B**	**4**	**4**		S. Draghici and I.K. Sethi	On the possibilities of the limited precision weights neural networks in classification problems	International Work-Conference on Artificial and Natural Neural Networks (LNCS 1240)	Lanzarote, Spain	4-6 Jun. 1997	753 - 762
	scitech	**D**	**1**	**0**		H.E. Makaruk	Computations of Entropy Bounds: Multidimensional Geometric Methods	Los Alamos National Laboratory LA-UR--97-4413	DOE, USA	Feb. 1998	1 - 10
	PhD	**D**	**1**	**0**		D. Braendler	Implementing Neural Hardware with On Chip Training on Field Programmable Gate Arrays	Swinburne University of Technology	Melbourne, Australia	Feb. 2002	1 - 312
	PhD	**D**	**1**	**0**		J.M.F. dos Santos	Data Classification with Neural Networks and Entropic Criteria	University of Porto	Porto, Portugal	Jan. 2007	1 - 212
7.00			**7**	**4**	**4.00**						
C057	**SOCO'97**					**V. Beiu, and S. Draghici**	**Limited Weights Neural Networks – Very Tight Entropy Based Bounds**	**ICSC International Symposium on Soft Computing**	**Nîmes, France**	**17-19 Sept. 1997**	**111 - 118**
	scitech	**D**	**1**	**0**		H.E. Makaruk	Computations of Entropy Bounds: Multidimensional Geometric Methods	Los Alamos National Laboratory LA-UR--97-4413	DOE, USA	Feb. 1998	1 - 10
	Journal	**B**	**4**	**4**		B.M. Wilamowski et al.	VLSI Implementation of Neural Networks	**International Journal of Neural Systems**	Vol. 10, No. 3	Jun. 2000	191 - 197
	Journal	**A**	**8**	**8**		S. Draghici	On the Capabilities of Neural Networks Using Limited Precision Weights	**Neural Networks**	Vol. 15, No. 3	Apr. 2002	395 - 414
13.00			**13**	**12**	**12.00**						
C060	**ANNIE-97**					**S. Draghici, V. Beiu, and I.K. Sethi**	**A VLSI Optimal Constructive Algorithm**	**International Conference on Artificial Neural Networks in Engineering**	**St. Louis, MI, USA**	**9-12 Nov. 1997**	**145 - 151**
	IWANN-99	**B**	**4**	**4**		S. Draghici	On the Computational Power of Limited Precision Weights Neural Networks for Classification Problems: How to Calculate the Weight Range so that a Solution Will Exist	International Work-Conference on Artificial Neural Networks (LNCS 1606)	Alicante, Spain	2-4 Jun. 1999	401 - 412
	IJCNN-99	**A**	**8**	**8**		S. Draghici	Some New Results on the Capabilities of Integer Weights Neural Networks in Classification Problems	IEEE International Joint Conference on Neural Networks	Washington, DC, USA	10-16 Jul. 1999	519 - 524
	IJCNN-99	**A**	**8**	**8**		S. Draghici and D.A. Miller	A VLSI Neural Network Classifier Based on Integer-Valued Weights	IEEE International Joint Conference on Neural Networks	Washington, DC, USA	10-16 Jul. 1999	2419 -2424
	Journal	**B**	**4**	**4**		S. Draghici	Neural Networks in Analog Hardware -- Design and Implementation Issues	**International Journal of Neural Systems**	Vol. 10, No. 1	Feb. 2000	19 - 42

	Journal	**A**	**8**	**8**		S. Draghici	The Constraint Based Decomposition (CBD) Training Architecture	**Neural Networks**	Vol. 14, No. 4-5	May 2001	527 - 550
	Journal	**A**	**8**	**8**		D. Braendler et al.	Deterministic Bit-Stream Digital Neurons	**IEEE Transactions on Neural Networks**	Vol. 13, Nov. 6	Nov. 2002	1514 - 1525
	PhD	**D**	**1**	**0**		D. Braendler	Implementing Neural Hardware with On Chip Training on Field Programmable Gate Arrays	Swinburne University of Technology	Melbourne, Australia	Feb. 2002	1 - 312
	Journal	**A**	**8**	**8**		S. Draghici	On the Capabilities of Neural Networks Using Limited Precision Weights	**Neural Networks**	Vol. 15, No. 3	Apr. 2002	395 - 414
49.00			**49**	**48**	**48.00**						

C061	**NOLTA-97**					**V. Beiu, and H.E. Makaruk**	**Computing Volumes of n-Dimensional Complexes**	**International Symposium on Nonlinear Theory and Its Applications**	**Honolulu, HI, USA**	**29 Nov. - 3 Dec. 1997**	**417 - 420**
	scitech	**D**	**1**	**0**		H.E. Makaruk	Computations of Entropy Bounds: Multidimensional Geometric Methods	Los Alamos National Laboratory LA-UR--97-4413	DOE, USA	Feb. 1998	1 - 10
1.00			**1**	**0**	**0.00**						

C062	**SBRN-97**					**V. Beiu, S. Draghici, and H.E. Makaruk**	**On Limited Fan-in Optimal Neural Networks**	**IEEE Brazilian Symposium on Neural Networks**	**Goiania, Brazil**	**3-5 Dec. 1997**	**19 - 30**
	springer	**D**	**1**	**0**		S. Draghici	On the Complexity of VLSI-friendly Neural Networks for Classification Problems	Biennial Conference of the Canadian Society for Computational Studies of Intelligence (LNCS 1418)	Vancouver, Canada	18-20 Jun. 1998	285 - 297
	IJCNN-98	**A**	**8**	**8**		S. Draghici	Using Information Entropy Bounds to Design VLSI Friendly Neural Networks	IEEE International Joint Conference on Neural Networks	Ankorage, AK, USA	4-9 May 1998	547 - 552
	scitech	**D**	**1**	**0**		H.E. Makaruk	Computations of Entropy Bounds: Multidimensional Geometric Methods	Los Alamos National Laboratory LA-UR--97-4413	DOE, USA	Feb. 1998	1 - 10
	IJCNN-99	**A**	**8**	**8**		S. Draghici	Some New Results on the Capabilities of Integer Weights Neural Networks in Classification Problems	IEEE International Joint Conference on Neural Networks	Washington, DC, USA	10-16 Jul. 1999	519 - 524
	Journal	**B**	**4**	**4**		S. Draghici	Neural Networks in Analog Hardware -- Design and Implementation Issues	**International Journal of Neural Systems**	Vol. 10, No. 1	Feb. 2000	19 - 42
	PhD	**D**	**1**	**0**		J. Yang	In-The-Loop Training of a VLSI Implementation of a Smart Sensor with Low Resolution Programmable Digital Weights	University of Windsor	Windsor, ON, Canada	May 2000	1 - 217
	PhD	**D**	**1**	**0**		D. Braendler	Implementing Neural Hardware with On Chip Training on Field Programmable Gate Arrays	Swinburne University of Technology	Melbourne, Australia	Feb. 2002	1 - 312
	Journal	**A**	**8**	**8**		S. Draghici	On the Capabilities of Neural Networks Using Limited Precision Weights	**Neural Networks**	Vol. 15, No. 3	Apr. 2002	395 - 414
	Journal	**A**	**8**	**8**		S. Aunet et al.	Real-Time Reconfigurable Linear Threshold Elements Implemented in Floating-Gate CMOS	**IEEE Transactions on Neural Networks**	Vol. 14, No. 5	Sept. 2003	1244 - 1256
40.00			**40**	**36**	**36.00**						

C064	**EIS-98**					**V. Beiu**	**How to Build VLSI-Efficient Neural Chips**	**ICSC International Symposium on Engineering of Intelligent Systems**	**Tenerife, Spain**	**9-13 Feb. 1998**	**66 - 75**
	CiteSeerX	**D**	**1**	**0**		R.E. Haskell	Neuro-Fuzzy Classification and Regression Trees	International Conference on Applications of Fuzzy Systems & Soft Computing	Wiesbaden, Germany	5-7 Oct. 1998	1 - 8
	Journal	**A**	**8**	**8**		D. Braendler et al.	Deterministic Bit-Stream Digital Neurons	**IEEE Transactions on Neural Networks**	Vol. 13, Nov. 6	Nov. 2002	1514 - 1525
	springer	**D**	**1**	**0**		F. Temurtas et al.	A Study on Neural Networks Using Taylor Series Expansion of Sigmoid Activation Function	International Conference on Computational Science and Its Applications (LNCS 3046)	Assisi, Italy	14-17 May 2004	389 - 397

	PhD	**D**	**1**	**0**		L. Brunelli	Abordagem para Reducao de Complexidade de RNA usando Reconfiguracao Dinamica	Universidade Federal de Campina Grande	Campina Grande, Paraiba, Brasil	Feb. 2005	1 - 184
	springer	**D**	**1**	**0**		A. Deshmukh et al.	Binary Neural Networks -- A CMOS Design Approach	Knowledge-Based Intelligent Information and Engineering Systems (LNAI 3681)	Melbourne, Australia	14-16 Sept. 2005	1291 - 1296
	CiteSeerX	**D**	**1**	**0**		C. S. Rai and A. P. Singh	A Review of Implementation Techniques for Artificial Neural Networks	University School of Information Technology, GGS Indraprastha University	Delhi, India	2006	1 - 7
	ieee	**D**	**1**	**0**		U. Farooq et al.	A Low Cost Microcontroller Implementation of Neural Network	IEEE International Conference on Computer and Automation	Singapore	26-28 Feb.	592 - 597
	Journal	**B**	**4**	**4**		J. Misra and I. Saha	Artificial Neural Networks in Hardware: A Survey of Two Decades of Progress	**Neurocomputing**	Vol. 74, No. 1-3	Dec. 2010	239 - 255
18.00			**18**	**12**	**12.00**						
C065	**IJCNN-98**					**V. Beiu, and H.E. Makaruk**	**Small Fan-In Is Beautiful**	**IEEE International Joint Conference on Neural Networks**	**Anchorage, AL, USA**	**4-9 May 1998**	**1321 - 1326**
	PhD	**D**	**1**	**0**		V. Annampedu	Nanotechnology Architectures for Pattern Matching (UMI 3270646)	Lehigh University	Bethlehem, PA, USA	2007	1 - 179
	Journal	**A**	**8**	**8**		V. Annampedu and M.D. Wagh	Decomposition of Threshold Functions into Bounded Fan-in Threshold Functions	**Information and Computation**	Vol. 227	Jun. 2013	84 - 101
9.00			**9**	**8**	**8.00**						
C070	**NC-98**					**V. Beiu**	**2D Neural Hardware vs 3D Biological Ones**	**ICSC/IFAC International Symposium on Neural Computations**	**Vienna, Austria**	**23-25 Sept. 1998**	**37 - 45**
	PhD	**D**	**1**	**0**		J.P. Neto	Construção Modular de Redes Neuronais Recorrentes Analógicas	University of Lisbon	Lisbon, Portugal	Dec. 2002	1 - 212
	ESANN-09	**B**	**4**	**4**		J. Partzsch and R. Schuffny	On the Routing Complexity of Neural Network Models -- Rent's Rule Revisited	European Symposium on Artificial Neural Networks	Bruges, Belgium	22-24 Apr. 2009	595 - 600
5.00			**5**	**4**	**4.00**						
C072	**SBRN-98**					**V. Beiu**	**On Kolmogorov's Superposition and Boolean Functions**	**IEEE Brazilian Symposium on Neural Networks**	**Belo Horizonte, Brazil**	**9-11 Dec. 1998**	**55 - 60**
	Book	**A**	**8**	**8**		D.P. Mandic and J.A. Chambers	Recurrent Neural Networks for Prediction: Learning Algorithms, Architectures and Stability	John Wiley & Sons	978-0-471-49517-8	Aug. 2001	1 - 308
	PhD	**D**	**1**	**0**		J. Braun	An Application of Kolmogorov's Superposition Theorem to Function Reconstruction in Higher Dimensions	University of Bonn	Bonn, Germany	Nov. 2009	1 - 185
9.00			**9**	**8**	**8.00**						
C074	**MWSCAS-00**					**V. Beiu**	**Ultra-Fast Noise Immune CMOS Threshold Gates**	**IEEE Midwest Symposium on Circuits and Systems**	**Lansing, MI, USA**	**8-11 Aug. 2000**	**1310 - 1313**
	Journal	**A**	**8**	**8**		S. Draghici	On the Capabilities of Neural Networks Using Limited Precision	**Neural Networks**	Vol. 15, No. 3	Apr. 2002	395 - 414
	ieee	**D**	**1**	**0**		V. Brea et al.	Robustness Improvement in Binary Cellular Non-linear Network	IEEE European Conference on Circuit, Theory and Design	Cork, Ireland	Aug. 29 - Sep.	149 - 152
	Journal	**B**	**4**	**4**		R. Zhang et al.	Threshold Network Synthesis and Optimization and Its Application to Nanotechnologies	**IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**	Vol. 24, No. 1	Jan. 2005	107 - 118
	PhD	**D**	**1**	**0**		R. Zhang	Computer-Aided Design Algorithm and Tools for Nanotechnologies	EE Department, Princeton University	Princeton, NJ, USA	Nov. 2006	1 - 157
14.00			**14**	**12**	**12.00**						

C075	CAS-00					V. Beiu	High-Speed Noise Robust Threshold Gates	IEEE International Semiconductor Conference	Sinaia, Romania	10-14 Oct. 2000	79 - 82
	Journal	A	8	8		S. Draghici	On the Capabilities of Neural Networks Using Limited Precision Weights	Neural Networks	Vol. 15, No. 3	Apr. 2002	395 - 414
8.00			8	8	8.00						
C076	CSCS-13					V. Beiu	On VLSI-Optimal Neural Computations	International Conference on Control Systems and Computer Science	Bucharest, Romania	31 May - 3 Jun. 2001	450 - 455
	Journal	A	8	8		S. Draghici	On the Capabilities of Neural Networks Using Limited Precision Weights	Neural Networks	Vol. 15, No. 3	Apr. 2002	395 - 414
8.00			8	8	8.00						
C077	IJCNN-01					V. Beiu	On Higher Order Noise Immune Perceptrons	IEEE International Joint Conference on Neural Networks	Washington, DC, USA	14-19 Jul. 2001	246 - 251
	Journal	A	8	8		S. Draghici	On the Capabilities of Neural Networks Using Limited Precision Weights	Neural Networks	Vol. 15, No. 3	Apr. 2002	395 - 414
8.00			8	8	8.00						
C082	NCI-03					R. Andonie, L.M. Sasu, and V. Beiu	A Modified Fuzzy ARTMAP Architecture for Incremental Learning Function Approximation	International Conference on Neural Networks and Computational Intelligence	Cancun, Mexico	19-21 May 2003	124 - 129
	ESANN-04	B	4	4		R. Andonie and L. Sasu	Convergence Properties of Fuzzy ARTMAP Network	European Symposium on Artificial Neural Networks	Bruges, Belgium	28-30 Apr. 2004	495 - 500
	springer	C	2	0		D. Wang et al.	Applying Neural Network to Reinforcement Learning in Continuous Spaces	International Symposium on Neural Networks (LNCS 3496)	Chongqing, China	2 May 2005	621 - 626
	Journal	A	8	8		R. Andonie and L.M. Sasu	Fuzzy ARTMAP with Input Relevances	IEEE Transactions on Neural Networks	Vol. 17, No. 4	Jul. 2006	929 - 941
	SMC-06	B	4	4		H.S. Mohammed et al.	Comparison of Ensemble Techniques for Incremental Learning of New Concept Classes under Hostile Non-stationary Environments	IEEE International Conference on Systems, Man, and Cybernetics	Taipei, Taiwan	8-11 Oct. 2006	4838 - 4844
	PhD	D	1	0		L.M. Sasu	Computational Intelligence Techniques in Data Mining	Technical University of Brasov	Brasov, Romania	11 Sept. 2006	1 - 136
	ieee	D	1	0		R. Andonie et al.	A New Fuzzy ARTMAP Approach for Predicting Biological Activity of Potential HIV-1 Protease Inhibitors	IEEE International Conference on Bioinformatics and Biomedicine	San Jose, CA, USA	2-7 Nov. 2007	56 - 61
	springer	D	1	0		L. Cervantes et al.	Agent-Based Approach to Distributed Ensemble Learning of Fuzzy ARTMAP Classifiers	First KES International Symposium Agent and Multi-Agent Systems: Technologies and Applications (LNCS 4496)	Wroclaw, Poland	31 May - 1 Jun. 2007	805 - 814
	Journal	A	8	8		L.M. Sasu and R. Andonie	Bayesian ARTMAP for Regression	Neural Networks	Vol. 46	Oct. 2013	23 - 31
29.00			29	24	24.00						
C083	IWANN-03					S. Tatapudi, and V. Beiu	Split-Precharge Differential Noise-Immune Threshold Logic Gate	International Work-Conference on Artificial Neural Networks	Menorca, Spain	3-6 Jun. 2003	49 - 56
	PhD	D	1	0		S.B. Tatapudi	A High Performance Low Power Mesochronous Pipeline Architecture for Computer Systems	Department of CE, Washington State University	Pullman, WA, USA	May 2006	1 - 110
	PhD	D	1	0		I.V. Potapov	Models, methods and objectives of the application of reliability theory neurocomputing systems	Novosibirsk State University	Novosibirsk, Russia	2010	1 - 348
	Journal	B	4			A. Mukati	A Survey of Memory Error Correcting Techniques for Improved Reliability	Journal of Network and Computer Applications	Vol. 34, No. 2	Mar. 2011	517 - 522

	ProQuest	D	1	0		A.P. James et al.	Threshnomics: An Introduction to Threshold Logic in Algorithms and Circuits	**Journal of Computer Science Systems Biology**	Vol. 7, No. 6	Jul. 2014	235 - 240
7.00			**7**	**0**	**0.00**						
C084	**ICANN-03**					**V. Beiu, J.M. Quintana, and M.J. Avedillo**	**Review of Capacitive Threshold Gate Implementations**	**International Conference on Artificial Neural Networks**	**Istanbul, Turkey**	**26-29 Jun. 2003**	**737 - 744**
	spie	D	1	0		K. Rajagopalan et al.	On-the-Fly Reconfigurable Logic	SPIE International Symposium Smart Structures, Devices, and Systems	Sydney, Australia	13 Dec. 2004	101 - 109
	acm	D	1	0		S. Maltabas et al.	Varicap Threshold Logic	ACM Great Lakes Symposium on VLSI	Boston, MA, USA	10-12 May 2009	239 - 244
	ieee	D	1	0		O.K. Ekekon et al.	Power Minimization Methodology for VCTL Topologies	IEEE International SOC Conference	Las Vegas, NV, USA	27-29 Sept. 2010	330 - 333
	ieee	D	1	0		M. Nikodem and M.A. Bawiec	Logic Circuit Synthesis Using Threshold Gates Based on Nanodevices with Negative Differential Resistance Property	IEEE International Conference on Nanotechnology	Seoul, Korea	17-20 Aug. 2010	227 - 232
	ieee	D	1	0		M. Nikodem et al.	Synthesis of Generalised Threshold Gates and Multi Threshold Threshold Gates	IEEE International Conference on Systems Engineering	Las Vegas, NV, USA	16-18 Aug. 2011	463 - 464
	ieee	D	1	0		F. Ercan and A. Muhtaroglu	Comparative power-delay performance analysis of threshold logic technologies	IEEE International Conference on Energy Aware Computing Systems & Applications (ICEAC)	Cairo, Egypt	24-26 Mar. 2015	7352166 (1 - 4)
6.00			**6**	**0**	**0.00**						
C085	**ICANN-03**					**V. Beiu**	**Constructive Threshold Logic Addition – A Synopsis of the Last Decade**	**International Conference on Artificial Neural Networks**	**Istanbul, Turkey**	**26-29 Jun. 2003**	**745 - 752**
	spie	D	1	0		K. Rajagopalan et al.	On-the-Fly Reconfigurable Logic	SPIE International Symposium Smart Structures, Devices, and Systems	Sydney, Australia	13 Dec. 2004	101 - 109
1.00			**1**	**0**	**0.00**						
C086	**UGIM-03**					**Z. Zhou, D.J. Betwoski, X. Li, G. La Rue, and V. Beiu**	**High Performance Direct Digital Frequency Synthesizers**	**Biennial University/Government/Industry Microelectronics Symposium**	**Boise, ID, USA**	**30 Jun. - 2 Jul. 2003**	**368 - 369**
	PhD	D	1	0		Z. Zhou	Non-linear D/A Converters for Direct Digital Frequency Synthesizers	Department of EE, Washington State University	Pullman, WA, USA	Aug. 2006	1 - 85
0.33			**1**	**0**	**0.00**						
C087	**SCS-03**					**V. Beiu, J.M. Quintana, M.J. Avedillo, and R. Andonie**	**Differential Implementations of Threshold Logic Gates**	**IEEE International Symposium on Signal, Circuits and Systems**	**Iaşi, Romania**	**10-11 Jul. 2003**	**489 - 492**
	acm	D	1	0		T. Gowda et al.	Combinational Equivalence Checking for Threshold Logic Circuits	ACM International Great Lakes Symposium on VLSI	Stresa, Italy	11-13 Mar. 2007	102 - 107
	acm	D	1	0		S. Maltabas et al.	Varicap Threshold Logic	ACM Great Lakes Symposium on VLSI	Boston, MA, USA	10-12 May 2009	239 - 244
	acm	D	1	0		A.K. Palaniswamy et al.	A Fault Tolerant Threshold Logic Gate Design	WSEAS International Conference on Circuits	Rodos, Greece	22-24 Jul. 2009	162 - 167
	ieee	D	1	0		O.K. Ekekon et al.	Power Minimization Methodology for VCTL Topologies	IEEE International SOC Conference	Las Vegas, NV, USA	27-29 Sept. 2010	330 - 333

	acm	D	1	0		A.K. Palaniswamy et al.	Scalable Identification of Threshold Logic Functions	ACM Great Lakes Symposium on VLSI	Providence, RI, USA	16-18 May 2010	269 - 273
	Journal	B	4	4		A.K. Palaniswamy and S. Tragoudas	An Efficient Heuristic to Identify Threshold Logic Functions	**ACM Journal on Emerging Technologies in Computing**	Vol. 8, No. 3	Aug. 2012	19 (1 - 17)
	ProQuest	D	1	0		A.P. James et al.	Threshnomics: An Introduction to Threshold Logic in Algorithms and Circuits	**Journal of Computer Science Systems Biology**	Vol. 7, No. 6	Jul. 2014	235 - 240
	Journal	B	4	4		A.K. Palaniswamy and S. Tragoudas	Improved Threshold Logic Synthesis Using Implicant-Implicit Algorithms	**ACM Journal on Emerging Technologies in Computing Systems**	Vol. 10, No. 3	Apr. 2014	21 (1 - 32)
	ieee	D	1	0		A.K. Palaniswamy et al.	ATPG for Transition Faults of Pipelined Threshold Logic Circuits	IEEE International Conference on Design & Technology of Integrated Systems In Nanoscale Era	Santorini, Greece	May 2014	6850662 (1 - 5)
	ieee	D	1	0		F. Ercan and A. Muhtaroglu	Comparative power-delay performance analysis of threshold logic technologies	IEEE International Conference on Energy Aware Computing Systems & Applications (ICEAC)	Cairo, Egypt	24-26 Mar. 2015	7352166 (1 - 4)
8.00			**16**	**8**	**4.00**						

C088	**IJCNN-03**					**V. Beiu**	**A Survey of Perceptron Circuit Complexity Results**	**IEEE International Joint Conference on Neural Networks**	**Portland, OR, USA**	**20-24 Jul. 2003**	**989 - 994**
	PhD	D	1	0		L. Brunelli	Abordagem para Reducao de Complexidade de RNA usando Reconfiguracao Dinamica	Universidade Federal de Campina Grande	Campina Grande, Paraiba, Brasil	Feb. 2005	1 - 184
	IJCNN-05	A	8	8		L. Brunelli et al.	A Novel Approach to Reduce Interconnect Complexity in ANN Hardware Implementation	IEEE International Joint Conference on Neural Networks	Montreal, Canada	31 Jul. - 4 Aug. 2005	2861- 2866
	Book	B	4	4		K.-L. Du and M.N.S. Swamy	Neural Networks in a Softcomputing Framework	Springer	London, UK	May 2006	1 - 566
	PhD	D	1	0		M. He	Contribution à l'étude de l'impact des nanotechnologies sur les architectures : Apprentissage d'inspiration neuronale de fonctions logiques pour circuits programmables	Université de Paris Sud XI	Orsay, France	17 Dec. 2008	1 - 159
	Chp. 23	B	4	4		K.-L. Du and M.N.S. Swamy	Neural Circuits and Parallel Implementation	In K.-L. Du and M.N.S. Swamy "Neural Networks and Statistical Learning"	Springer	Dec. 2013	705 - 725
	ieee	D	1	0		N. Kulkarni et al.	A fast, energy efficient, field programmable threshold-logic array	IEEE International Conference on Field-Programmable Technology (FPT)	Shanghai, China	10-12 Dec. 2014	300 - 305
	ieee	D	1	0		J. Yang et al.	Dynamic and Leakage Power Reduction of ASICs Using Configurable Threshold Logic Gates	IEEE Custom Integrated Circuits Conference (CICC)	San Jose, CA,USA	28-30 Sept. 2015	7338369 (1 - 4)
	Journal	B	4	4		N. Kulkarni et al.	Reducing Power, Leakage, and Area of Standard-Cell ASICs Using Threshold Logic Flip-Flops	**IEEE Transactions on Very Large Scale Integration (VLSI) Systems**	Vol. 24, No. 9	Sept. 2016	2873 - 2886
24.00			**24**	**20**	**20.00**						

C089	**IJCNN-03**					**R. Andonie, L. Sasu, and V. Beiu**	**Fuzzy ARTMAP with Relevance Factor**	**IEEE International Joint Conference on Neural Networks**	**Portland, OR, USA**	**20-24 Jul. 2003**	**1975 - 1980**
	ESANN-05	B	4	4		R. Andonie and L. Sasu	Convergence Properties of Fuzzy ARTMAP Network	European Symposium on Artificial Neural Networks	Bruges, Belgium	28-30 Apr. 2004	495 - 500
	PhD	D	1	0		L.M. Sasu	Computational Intelligence Techniques in Data Mining	Technical University of Brasov	Brasov, Romania	11 Sept. 2006	1 - 136

5.00			5	4	4.00							
C090	ICNNSP-03					D.J. Betowski, and V. Beiu	Considerations for Phase Accumulator Design for Direct Digital Frequency Synthesizers	IEEE International Conference on Neural Networks and Signal Processing	Nanjing, China	14-17 Dec. 2003	176 - 179
	Journal	C	2	0		E. Merlo and K.-H. Baek	High-Speed Low-Power Small-Area Accumulator Designs for Direct Digital Frequency Synthesizers	**IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences**	Vol. E88-A, No. 5	May 2005	1373 - 1378
	ieee	D	1	0		W. Li and J. Zhang	Research of Parameter Adjustable Harmonic Signal Generator Based on DDS	IEEE International Colloquium on Computing, Communication, Control, and Management	Guangzhou, China	3-5 Aug. 2008	88 - 91
	PhD	D	1	0		S. Kim	High-Speed Analog-to-Digital Converters for Modern Satellite Receivers: Design Verification Test and Sensitivity Analysis (UMI 3297408)	University of Maryland	College Park, MD, USA	2008	1 - 271
	US 7,565,392	D	1	0		S. Turner	Single-Level Parallel-Gated Carry/Majority Circuits and System Therefrom	BAE Systems International and Electronic Systems Integration Inc.	Washington, DC, USA	21 Jul. 2009	1 - 15
	ieee	D	1	0		Z. Zhang and F. Dong	A Harmonic Signal Generator Based on DDS and SOPC	IEEE Chinese Control and Decision Conference	Xuzhou, China	26-28 May 2010	1542 - 1547
	PhD	D	1	0		C.-H. Lin	Look-up table based on the sine wave symmetry and second-order algorithms for high-performance direct digital frequency synthesizer design	National Changhua University of Education	Taiwan	2011	1 - 98
	ieee	D	1	0		S. Liu et al.	An Experimental Research on Acoustic Emission Technology Induced by Eddy Current	IEEE International Conference on Electric Power Equipment – Switching Technology	Xi'an, China	23-27 Oct. 2011	573 - 576
	ieee	D	1	0		P. Yuan et al.	Design of Digital Signal Generator of Radio Navigation Based on	IEEE International Conference on Communication Software &	Xi'an, China	27-29 May	379 - 382
	CiteSeerx	D	1	0		S.V. Devika et al.	High Speed and Dynamic Switching Type Signal Generation on	**International Journal of Engineering Research and**	Vol. 2, No. 2	Mar. - Apr.	241 - 246
	Journal	B	4	4		S. Liu et al.	Power Source of Electromagnetically Induced Acoustic Emission Based on DDS	**Transactions of China Electrotechnical Society**	Vol. 27, No. 6	Jun. 2012	6 - 11
	CiteSeerX	D	1	0		S.M. Inthiyaz and B. Sumithra	FPGA Implementation of Radio Navigation Based on MicroBlaze	**International Journal of Engineering Research and Applications**	Vol. 3, No. 3	May - Jun. 2013	1032 - 1039
	Journal	D	1	0		S.H. Ibrahim et al.	Implementation of a 32-bit High Speed Phase Accumulator for Direct Digital Frequency Synthesizer	**Asian Journal of Scientific Research**	Vol. 7, No. 1	Jan. 2014	118 - 124
	spie	D	1	0		Z. Liu et al.	A Design of Three-stage Addressing Sweep Frequency Signal Generator	Applied Optics and Photonics China 2015: Image Processing and Analysis	Beijing, China	5-7 May 2015	http://dx.doi.org/10.1117/12.2199054
	spie	D	1	0		Z. Liu et al.	A Design of DDS Single-frequency Signal Generator Based on Phrase Jitter Technology to Reduce Scattering Noise	Applied Optics and Photonics China 2015: Image Processing and Analysis	Beijing, China	5-7 May 2015	http://dx.doi.org/10.1117/12.2199056
	ieee	D	1	0		S. Nazir et al.	Pipelined phase accumulator using han carlson adders and reduced pre-skewing flip-flops for DDFS	IEEE International SoC Design Conference (ISOCC)	Gyungju, South Korea	2-5 Nov. 2015	311 - 312
	ProQuest	D	1	0		G. Indhumathi and R. Seshasayanan	Periodic Wave Generation for Direct Digital Synthesization	**International Journal on Intelligent Electronics Systems**	Vol. 10, No.1	Jan. 2016	22 - 27
	US 9,244,483	D	1	0		A.N. Willson Jr.	Excess-Fours Processing in Direct Digital Synthesizer Implementations	**Pentomics, Inc.**	Washington, DC, USA	26 Jan. 2016	https://www.google.com/patents/US9244483
21.00			21	4	4.00						
C093	MWSCAS-03					M.H. Sulieman, and V. Beiu	Review of Recent Full Adders Implemented in Single Electron Technology	IEEE International Midwest Symposium on Circuit and Systems	Cairo, Egypt	27-30 Dec. 2003	872 - 875

	ProQuest	D	1	0		A. Sahafi et al.	CNFET Based Basic Gates and a Novel Full-Adder Cell	**International Journal of VLSI Design & Communication Systems**	Vol. 3, No. 3	Jun. 2012	11 - 19
1.00			1	0	0.00						
C094	**MWSCAS-03**					**V. Beiu, J.M. Quintana, M.J. Avedillo, and M.H. Sulieman**	**Threshold Logic – From Vacuum Tubes to Nanoelectronics**	**IEEE International Midwest Symposium on Circuit and Systems**	**Cairo, Egypt**	**27-30 Dec. 2003**	**930 - 935**
	cordis.eu	D	1	0		W. Prost	QUDOS Quantum Tunnelling Devices Technology on Silicon	Quantum Tunnelling Device Technology on Silicon	Brussels, Belgium	27 Oct. 2004	1 - 80
	acm	D	1	0		A.K. Palaniswamy et al.	A Fault Tolerant Threshold Logic Gate Design	WSEAS International Conference on Circuits	Rodos, Greece	22-24 Jul. 2009	162 - 167
	acm	D	1	0		A.K. Palaniswamy et al.	Scalable Identification of Threshold Logic Functions	ACM Great Lakes Symposium on VLSI	Providence, RI, USA	16-18 May 2010	269 - 273
	Journal	**B**	**4**	**4**		A.K. Palaniswamy and S. Tragoudas	An Efficient Heuristic to Identify Threshold Logic Functions	**ACM Journal on Emerging Technologies in Computing**	Vol. 8, No. 3	Aug. 2012	19 (1 - 17)
3.50			7	4	2.00						
C095	**MWSCAS-03**					**V. Beiu, D.J. Betowski, and P.-S. Wu**	**Over 100 dBc ROM-less Piecewise Non-linear Direct Digital Frequency Synthesizers**	**IEEE International Midwest Symposium on Circuit and Systems**	**Cairo, Egypt**	**27-30 Dec. 2003**	**760 - 763**
	Journal	**C**	**2**	**0**		E. Hertz et al.	Combining the Parabolic Synthesis Methodology with Second-Degree Interpolation	**Microprocessors and Microsystems**	Vol. 42	May 2016	142 - 155
2.00			2	0	0.00						
C096	**MWSCAS-03**					**V. Beiu**	**Threshold Logic Implementations – The Early Days**	**IEEE International Midwest Symposium on Circuit and Systems**	**Cairo, Egypt**	**27-30 Dec. 2003**	**1379 - 1383**
	ESANN-13	B	4	4		J.B. da Fonseca	Are Rosenblatt Multilayer Perceptrons More Powerfull than Sigmoidal Multilayer Perceptrons? From a Counter Example to a General Result	European Symposium on Artificial Neural Networks, Computational Intelligence and Machine Learning	Bruges, Belgium	Apr. 2013	345 - 350
	ieee	D	1	0		J. Das and S. Bhanja	A Novel Knowledge Module to Integrate Threshold Logic and Post-CMOS Technology into Undergraduate Logic Design Classroom	IEEE Interdisciplinary Engineering Design Education Conference (IEDEC)	Santa Clara, CA, USA	Mar. 2014	24-30
	ProQuest	D	1	0		A.P. James et al.	Threshnomics: An Introduction to Threshold Logic in Algorithms	**Journal of Computer Science Systems Biology**	Vol. 7, No. 6	Jul. 2014	235 - 240
6.00			6	4	4.00						
C098	**ISCAS-04**					**M.H. Sulieman, and V. Beiu**	**Characterization of a 16-bit Threshold Logic Single Electron Technology Adder**	**IEEE International Symposium on Circuits and Systems**	**Vancouver, Canada**	**23-26 May 2004**	**681 - 684**
	Journal	**D**	**1**	**0**		D. Samanta et al.	Design and Implementation of a Sequence Generator using Single Electron Device based Threshold Logic Gates	**Far East Journal of Electronics and Communications**	Vol. 1, No. 3	Dec. 2007	247 - 258
	Journal	**C**	**2**	**0**		W. Zhang and N.-J. Wu	Compact Non-binary Fast Adders Using Single-electron Devices	**Microelectronics Journal**	Vol. 40, No. 8	Aug. 2009	1244 - 1254
	ieee	D	1	0		N. Kulkarni et al.	A fast, energy efficient, field programmable threshold-logic array	IEEE International Conference on Field-Programmable Technology (FPT)	Shanghai, China	10-12 Dec. 2014	300 - 305
4.00			4	0	0.00						

C099	VLSI-04					V. Beiu, and M.H. Sulieman	Optimal Practical Perceptron Addition – Application to Single Electron Technology	International Multiconference VLSI-04	Las Vegas, NV, USA	21-25 Jun. 2004	541 - 547
	PhD	D	1	0		J. Sima	Neuronové Síte Jako Modely Analogových Výpoctu	Academy of the Czech Republic	Prague, Czech Republic	Apr. 2006	1 - 46
1.00			1	0	0.00						
C100	VLSI'04					D.J. Betowski, D. Dwyer, and V. Beiu	A Novel Segmented Parabolic Sine Approximation for Direct Digital Frequency Synthesizers	International Multiconference VLSI'04	Las Vegas, NV, USA	21-25 Jun. 2004	523 - 529
	Journal	A	8	8		C.Y. Kang and E.E. Swartzlander	Digit-Pipelined Direct Digital Frequency Synthesis Based on Differential CORDIC	IEEE Transactions on Circuit and Systems I	Vol. 53, No. 5	May 2006	1035 - 1044
8.00			8	8	8.00						
C101	IJCNN-04					J. Nyathi, V. Beiu, S. Tatapudi, and D.J. Betwoski	A Charge Recycling Differential Noise-Immune Perceptron	IEEE International Joint Conference on Neural Networks	Budapest, Hungary	25-29 Jul. 2004	1995 - 2000
	PhD	D	1	0		S.B. Tatapudi	A High Performance Low Power Mesochronous Pipeline Architecture for Computer Systems	Department of CE, Washington State University	Pullman, WA, USA	May 2006	1 - 110
0.50			1	0	0.00						
C102	IEEE-NANO-04					M.H. Sulieman, and V. Beiu	Design and Analysis of SET Circuits – Using MATLAB Modules and Simon	IEEE International Conference on Nanotechnology	Munich, Germany	17-19 Aug. 2004	618 - 621
	Journal	A	8	8		C. Chen	Reliability-Driven Gate Replication for Nanometer-Scale Digital Logic	IEEE Transactions on Nanotechnology	Vol. 6	May 2007	303 - 308
	Journal	A	8	8		C. Meenderinck and S. Cotofana	Computing Division using Single-Electron Tunneling Technology	IEEE Transactions on Nanotechnology	Vol. 6, No. 4	Jul. 2007	451 - 459
	acm	D	1	0		M.H. Sulieman	Reliability of single-electron logic gates	ACM Conference on Microelectronics, Nanoelectronics, Optoelectronics	Istanbul, Turkey	27-29 May 2007	50 - 53
	Journal	A	8	8		C. Chen and Y. Mao	A Statistical Reliability Model for Single-Electron Threshold Logic	IEEE Transactions on Electron Devices	Vol. 55, No. 6	Jun. 2008	1547 - 1553
	Journal	D	1	0		A.M. Hashim and G. Murugiah	Modeling and Characterization of Majority (MAJ) Type Single-Electron Full Adder Using Simon	Jurnal Teknologi	Vol. 49	Dec. 2008	107 - 116
	ieee	D	1	0		Y. Mao and C. Chen	Modeling Reliability for Single-Electron Tunneling Logic Gates	IEEE International Conference on Nanotechnology	Arlington, TX, USA	18-21 Aug. 2008	379 - 381
	ieee	D	1	0		M. Karimian et al.	A New SPICE Macro-Model for Simulation of Single Electron Circuits	IEEE International Conference on Microelectronics	Marrakech, Morocco	19-22 Dec. 2009	228 - 231
	ieee	D	1	0		M. Karimian et al.	An Improved Macro-model for Simulation of Single Electron Transistor (SET) using HSPICE	IEEE International Science and Technology for Humanity	Toronto, Canada	26-27 Sept. 2009	1000 - 1004
	PhD	D	1	0		M. Stanisavljević	On the Dependability of Nanoscale Circuits and Systems: Methodologies and Circuit Architectures	Ecole Polytechnique Federale de Lausanne	Lausanne, Switzerland	27 Mar. 2009	1 - 238
	Book	B	4	4		M. Stanisavljević et al.	Reliability of Nanoscale Circuits and Systems: Methodologies and Circuit Architectures	Springer	New York	2011	1 - 195

34.00			**34**	**28**	**28.00**						
C103	**IEEE-NANO-04**					**S. Roy, and V. Beiu**	**Multiplexing Schemes for Cost-Effective Fault-Tolerance**	**IEEE International Conference on Nanotechnology**	**Munich, Germany**	**17-19 Aug. 2004**	**589 - 592**
	semantic	**D**	**1**	**0**		D. Bhaduri and S. Shukla	Comparing Reliability-Redundancy Trade-offs for Two von Neumann Multiplexing Architectures	FERMAT Tech. Rep. 2005-01, VirginiaTech	Semantic Scholar, Allen Inst. AI	2005	1 - 22
	Journal	**A**	**8**	**8**		J.B. Gao et al.	Bifurcations and Fundamental Error Bounds for Fault-Tolerant Computations	**IEEE Transactions on Nanotechnology**	Vol. 4, No. 4	Jul. 2005	395 - 402
	springer	**D**	**1**	**0**		M. Stanisavljević et al.	A Methodology for Reliability Enhancement of Nanometer-scale Digital Systems Based on a-priori Functional Fault-tolerance Analysis	IFIP (International Federation for Information Processing) VLSI-SoC	Perth, Australia	17-19 Oct. 2005	111 - 125
	PhD	**D**	**1**	**0**		G.R. Roelke	Fault and Defect Tolerant Computer Architectures: Reliable Computing With Unreliable Devices	Air Force Institute of Technology	Wright-Patterson, OH, USA	Sept. 2006	1 - 421
	PhD	**D**	**1**	**0**		H. Naeimi	Reliable Integration of Terascale Systems with Nanoscale Devices	California Institute of Tecnology	Pasadena, CA, USA	4 Sept. 2007	1 - 181
	Journal	**A**	**8**	**8**		G.R. Roelke at al.	Analytical Models for the Performance of von Neumann Multiplexing	**IEEE Transactions on Nanotechnology**	Vol. 6, No. 1	Jan. 2007	75 - 89
	Journal	**A**	**8**	**8**		G.S. Snider	Self-organized Computation with Unreliable, Memristive Nanodevices	**Nanotechnology**	Vol. 18, No. 36	12 Sept. 2007	365202 (1 - 13)
	acm	**D**	**1**	**0**		M. Stanisavljević et al.	Design and Realization of a Fault-tolerant 90nm CMOS Cryptographic Engine Capable of Performing Under Massive Devect Density	ACM International Great Lakes Symposium on VLSI	Stresa, Italy	11-13 Mar. 2007	204 - 207
	ieee	**D**	**1**	**0**		M. Stanisavljević et al.	Case Study of Fault-Tolerant Architectures for 90nm Cryptographic Cores	IEEE Conference on PhD Research in Microelectronics and Electronics	Bordeaux, France	2-5 Jul. 2007	253 - 256
	springer	**D**	**1**	**0**		M. Stanisavljević et al.	A Methodology for Reliability Enhancement of Nanometer-scale Digital Systems Based on a-priori Functional Fault-tolerance Analysis	IFIP (International Federation for Information Processing) VLSI-SoC: From Systems to Silicon	Atlanta, GA, USA Springer -- Vol. 240	15-17 Oct. 2007	111 - 125
	ieee	**D**	**1**	**0**		M. Vural et al.	Fault Tolerance of Feed-forward Artificial Neural Network Architectures Targeting Nano-scale Implementations	IEEE Midwest Symposium on Circuits and System	Montreal, Canada	5-8 Aug. 2007	779 - 782
	PhD	**D**	**1**	**0**		H. Naeimi	Reliable Integration of Terascale Systems with Nanoscale Devices (UMI 3526020)	California Institute of Technology	Pasadena, CA, USA	24 Jan. 2008	1 - 172
	ISCAS-08	**C**	**2**	**0**		V. Puthucode and C. Chen	An Experimental Study on Multi-Island Structures for Single-Electron Tunneling Based Threshold Logic	IEEE International Symposium on Circuits and Systems	Seattle, WA, USA	18-21 May 2008	600 - 603
	Journal	**C**	**2**	**0**		K. Rathnakannan and P.V. Ranjan	Design and Modelling of Single Electron Transistor Based Reconfigurable Adder-Subtractor	**Journal of Nanoelectronics and Optoelectronics**	Vol. 3, No. 3	Dec. 2008	289 - 296
	Journal	**A**	**8**	**8**		M. Stanisavljević et al.	Optimization of Nanoelectronic Systems' Reliability under Massive Defect Density using Cascaded R-fold Modular Redundancy	**Nanotechnology**	Vol. 19, No. 46	19 Nov. 2008	465202 (1 - 9)
	PhD	**D**	**1**	**0**		M. Stanisavljević	On the Dependability of Nanoscale Circuits and Systems: Methodologies and Circuit Architectures	Ecole Polytechnique Federale de Lausanne	Lausanne, Switzerland	27 Mar. 2009	1 - 238
	Journal	**A**	**8**	**8**		M. Stanisavljević et al.	Optimization of the Averaging Reliability Technique Using Low Redundancy Factors for Nanoscale Technologies	**IEEE Transactions on Nanotechnology**	Vol. 8, No. 3	May 2009	379 - 390

	ieee	D	1	0		M. Stanisavljević et al.	Optimization of Nanoelectronic Systems Reliability Under Massive Defect Density Using Distributed R-fold Modular Redundancy (DRMR)	IEEE International Symposium on defect and Fault Tolerance in VLSI Systems	Chicago, IL, USA	7-9 Oct. 2009	340 - 348
	Book	**B**	**4**	**4**		M. Stanisavljević et al.	Reliability of Nanoscale Circuits and Systems: Methodologies and Circuit Architectures	Springer	New York	2011	1 - 195
	Chp. 18	**A**	**8**	**8**		M. Stanisavljević et al.	Reliability of Nanoelectrinic VLSI	In K. Iniewski (ed.): Advanced Circuits for Emerging Technologies	John Wiley	May 2012	463 - 482
	PhD	**D**	**1**	**0**		N. Aymerich	Variability-aware Architectures based on Hardware Redundancy for Nanoscale Reliable Computation	Universidad Politecnica de Catalunya	Barcelona, Spain	Dec. 2013	1 - 149
	Journal	**D**	**1**	**0**		D. Jose et al.	Reliability Improvement of Partitioned VLSI Systems for Fault Tolerance	**International Journal of Applied Engineering Research**	Vol. 10, No. 7	Jul. 2015	18151 - 18165
	Journal	**A**	**8**	**8**		W. Ibrahim	Identifying the Worst Reliability Input Vectors and the Associated Critical Logic Gates	**IEEE Transactions on Computers**	Vol. 65, No. 6	Jul. 2016	1748 - 1760
77.00			**77**	**60**	**60.00**						

C104	**IEEE-NANO-04**					**M.H. Sulieman, and V. Beiu**	**On Single Electron Technology Full Adders**	**IEEE International Conference on Nanotechnology**	**Munich, Germany**	**17-19 Aug. 2004**	**317 - 320**
	ieee	D	1	0		J. Han et al.	Reliability Modeling of Nanoelectronic Circuits	IEEE Conference on Nanotechnology	Nagoya, Japan	11-15 Jul. 2005	269 - 272
	ieee	D	1	0		D. Samanta et al.	SET Based Logic Realization of a Robust Spatial Domain Image Watermarking	IEEE International Conference on Electrical and Computer Engineering	Dhaka, Bangladesh	20-22 Dec. 2008	986 - 993
	Journal	**D**	**1**	**0**		M.R. Karimian et al.	A New SPICE Macro-model for the Simulation of Single Electron Circuits	**Journal of the Korean Physical Society**	Vol. 56, No. 4	Apr. 2010	1202 - 1207
	Journal	**B**	**4**	**4**		G. Deng and C. Chen	Hybrid CMOS-SET Arithmetic Circuit Design Using Coulomb Blockade Oscillation Characteristic	**Journal of Computational and Theoretical Nanoscience**	Vol. 8, No. 8	Aug. 2011	1520 - 1526
7.00			**7**	**4**	**4.00**						

C105	**IEEE-NANO-04**					**V. Beiu, U. Rückert, S. Roy, and J. Nvathi**	**On Nanoelectronic Architectural Challenges and Solutions**	**IEEE International Conference on Nanotechnology**	**Munich, Germany**	**17-19 Aug. 2004**	**628 - 631**
	Chp. 6	**B**	**4**	**4**		D. Bhaduri and S. Shukla	Tools and Techniques for Evaluating Reliability Trade-offs for Nano-Architectures	Chapter 6 in S. Shukla and I. Bahar (Eds.): "Nano, Quantum and Molecular Computing: Implications to High Level Design and Validation"	Springer	May 2004	157 - 211
	ieee	D	1	0		D. Bhaduri and S. Shukla	Reliability Evaluation of von Neumann Multiplexing Based Defect-tolerant Majority Circuits	IEEE International Conference on Nanotechnology	Munich, Germany	16-19 Aug. 2004	599 - 601
	IJCNN-04	A	8	8		J.G. Taylor	CHIMERA: Creating a New Geeration Chip by Brain Guidance	IEEE International Joint Conference on Neural Networks	Budapest, Hungary	25-29 Jul. 2004	1989 - 1994
	IWANN-05	B	4	4		R. Eickhoff and U. Rückert	Robustness of Radial Basis Functions	International Workshop on Artificial Neural Networks (LNCS 3512)	Barcelona, Spain	8-10 Jun. 2005	264 - 271
	ICANN-05	B	4	4		R. Eickhoff and U. Rückert	Tolerance of Radial Basis Functions against Stuck-At-Faults	International Conference on Artificial Neural Networks (LNCS 3697)	Warsaw, Poland	11-15 Sept. 2005	1003 - 1008
	SMC-05	B	4	4		R. Eickhoff and U. Rückert	Fault-Tolerance of Basis Function Networks using Tensor Product Stabilizers	IEEE International Conference on System, Man and Cybernetics	Honolulu, HI, USA	10-12 Oct. 2005	2144 - 2149
	Journal	**A**	**8**	**8**		Y. Qi et al.	Markov Chains and Probabilistic Computation — A General Framework for Multiplexed Nanoelectronic Systems	**IEEE Transactions on Nanotechnology**	Vol. 4, No. 2	Mar. 2005	194 - 205

	PhD	**D**	**1**	**0**	S. Venkataraman	Fabrication of Two-Dimensional and Three-Dimensional Photonic Crystal Devices for Applications in Chip-Scale Optical Interconnects (UMI 3200519)	University of Delaware	Newark, DE, USA	Fall 2005	1 - 196
	WCCI-06	**A**	**8**	**8**	R. Eickhoff et al.	SIRENS: A Simple Reconfigurable Neural Hardware Structure for Artificial Neural Network Implementations	IEEE World Congress on Computational Intelligence	Vancouver, Canada	16-21 Jul. 2006	2830 - 2837
	PhD	**D**	**1**	**0**	R. Eickhoff	Fehlertolerante Neuronale Netze zur Approximation von Funktionen	University of Paderborn	Paderborn, Germany	11 Jul. 2007	1 - 260
	IWANN-07	**B**	**4**	**4**	R. Eickhoff et al.	Neural Inspired Architectures for Nanoelectronics	International Work-conference on Artificial Neural Networks (LNCS 4507)	San Sebastian, Spain	20-22 Jun. 2007	414 - 421
	Journal	**A**	**8**	**8**	R. Eickhoff and U. Rückert	Robustness of Radial Basis Functions	**Neurocomputing**	Vol. 70, No. 16-18	Oct. 2007	2758 - 2767
	Journal	**C**	**2**	**0**	W. Ibrahim	A Novel EDA Tool for VLSI Test Vectors Management	**Journal of Electronic Testing**	Vol. 23, No. 5	Oct. 2007	421 - 434
	ieee	**D**	**1**	**0**	A. Sahafi and K. Navi	A Novel Single Electron Technology Cell Based on Majority Logic Gate	IEEE International Conference on Enabling Science and Nanotechnology	Johor Bahru, Malaysia	5-7 Jan. 2012	1 - 2
	ingenta	**D**	**1**	**0**	A. Sahafi et al.	An Efficient Versatile Logic Cell for Single-Electron Technology	**Quantum Matter**	Vol. 3, No. 1	Feb. 2014	57 - 60
	Journal	**C**	**2**	**0**	A.S. Narwariya and S. Akashe	Reduction of Leakage Power in Half- Subtractor using AVL Technique based on 45nm CMOS Technology	**International Journal of Computer Applications**	Vol. 111, No. 1	Feb. 2015	31 - 35
30.50			**61**	**52**	**26.00**					

C106	**ASAP-04**				**V. Beiu**	**A Novel Highly Reliable Low-Power Nano Architecture: When von Neumann Augments Kolmogorov**	**IEEE International Conference on Application-specific Systems, Architectures and Processors**	**Galveston, TX, USA**	**27-29 Sept. 2004**	**167 - 177**
	ifip	**D**	**1**	**0**	S. Aunet and Y. Berg	Three Sub-fJ Power-Delay-Product Subthreshold CMOS Gates	IFIP (International Federation for Information Processing) VLSI-SoC	Perth, Australia	17-19 Oct. 2005	465 - 470
	Chp. 18	**B**	**4**	**4**	S. Das et al.	Architectures and Simulations for Nanoprocessor Systems Integrated on the Molecular Scale	In G. Cuniberti, G. Fagas, and K. Richter (Eds.): "Introducing Molecular Electronics" (LNP 680)	Springer	Dec. 2005	479 - 512
	Journal	**A**	**8**	**8**	J.B. Gao et al.	Bifurcations and Fundamental Error Bounds for Fault-Tolerant Computations	**IEEE Transactions on Nanotechnology**	Vol. 4, No. 4	Jul. 2005	395 - 402
	ITRS-ERD-05	**D**	**1**	**0**	***	Emerging Research Devices -- International Technology Roadmap for Semiconductors	SEMATECH	Austin, TX, USA	2005	1 - 76
	Journal	**D**	**1**	**0**	C. Catley et al.	Predicting High-Risk Preterm Birth Using Artificial Neural Networks	**IEEE Transactions on Information Technology in Biomedicine**	Vol. 10, No. 3	Jul. 2006	540 - 549
	ieee	**D**	**1**	**0**	D. Zhou and M. Frize	Predicting Probability of Mortality in the Neonatal Intensive Care Unit	IEEE Conference Engineering in Medicine and Biology Society	New York, NY, USA	30 Aug. - 3 Sept. 2006	2308 - 2311
	PhD	**D**	**1**	**0**	C.A. Catley	An Integrated Hybrid Data Mining System for Preterm Birth Risk AssesmentBased on a 'Semantic Web Services for Healthcare' Framework	Carleton University	Ottawa, ON, Canada	2007	1 - 252
	Journal	**A**	**8**	**8**	G.S. Snider	Self-organized Computation with Unreliable, Memristive Nanodevices	**Nanotechnology**	Vol. 18, No. 36	12 Sept. 2007	365202 (1 - 13)
	ITRS-ERD-07	**D**	**1**	**0**	***	Emerging Research Devices -- International Technology Roadmap for Semiconductors	SEMATECH	Austin, TX, USA	2007	1 - 55
	Journal	**A**	**8**	**8**	R. Cavin et al.	Emerging Research Architectures	**IEEE Computer**	Vol. 41, No. 5	May 2008	33 - 37
	PhD	**D**	**1**	**0**	M. He	Contribution à l'étude de l'impact des nanotechnologies sur les architectures : Apprentissage d'inspiration neuronale de fonctions logiques pour circuits programmables	Université de Paris Sud XI	Orsay, France	17 Dec. 2008	1 - 159
	ieee	**D**	**1**	**0**	G.S. Snider	Spike-Timing-Dependent Learning in Memresistive Nanodevices	ACM/IEEE International Conference on Nano Architectures	Anaheim, CA, USA	12-13 Jun. 2008	85 - 92
	ieee	**D**	**1**	**0**	A. Beg and W. Ibrahim	Relating Reliability to Circuit Topology	IEEE North-East Workshop on Circuits and Systems	Toulouse, France	28 Jun. - 1 Jul. 2009	5290421 (1-4)

	ieee	D	1	0		J. Flak and M. Laiho	Implementation Aspects of Fault-Tolerant Logic Built with Single-Electron Devices	IEEE Norchip International Conference	Trondheim, Norway	16-17 Nov. 2009	5397816 (1-4)
	Journal	**B**	**4**	**4**		J. Flak and M. Laiho	Fault-Tolerant Programmable Logic Array for Nanoelectronics	**International Journal of Circuit Theory and Applications**	Vol. 40, No. 12	Dec. 2012	1233 - 1247
42.00			**42**	**32**	**32.00**						

C107	**IWANN-05**					**V. Beiu, A. Zawadzki, R. Andonie, and S. Aunet**	**Using Kolmogorov Inspired Gates for Low Power Nanoelectronics**	**International Work-Conference on Artificial Neural Networks**	**Barcelona, Spain**	**8-10 Jun. 2005**	**438 - 445**
	Journal	**C**	**2**	**0**		G. Bezulski	Evaluating Sprecher's Algorithm Performance	**Mathematical Economics**	Vol. 11, No. 4	2007	71 - 84
	dagstuhl	D	1	0		F. Ablayev and S. Ablayeva	A Communication Complexity Approach to the Superposition Problem	In M. Agrawal et al. (Eds.): "Algebric Methods in Computational Complexity"	Wadern, Germany	11-16 Oct. 2009	1 - 4
	PhD	D	1	0		J. Braun	An Application of Kolmogorov's Superposition Theorem to Function Reconstruction in Higher Dimensions	University of Bonn	Bonn, Germany	Nov. 2009	1 - 185
	Journal	**B**	**4**	**4**		F. Ablayev and S. Ablayeva	A Communication Approach to the Superposition Problem	**Fundamenta Informaticae**	Vol. 104, No. 3	Aug. 2010	185 - 200
4.00			**8**	**4**	**2.00**						

C108	**IWANN-05**					**V. Beiu, A. Djupdal, and S. Aunet**	**Ultra Low-Power Neural Inspired Addition – When Serial Might Outperform Parallel Architectures**	**International Work-Conference on Artificial Neural Networks**	**Barcelona, Spain**	**8-10 Jun. 2005**	**486 - 493**
	ifip	D	1	0		S. Aunet and Y. Berg	Three Sub-fJ Power-Delay-Product Subthreshold CMOS Gates	IFIP (International Federation for Information Processing) VLSI-SoC	Perth, Australia	17-19 Oct. 2005	465 - 470
	PhD	D	1	0		P. Beckett	Predicting Power Scalability in a Reconfigurable Platform	School of ECE, Royal Melbourne Institute of Technology	Melbourne, Australia	Aug. 2007	1 - 244
	Journal	**A**	**8**	**8**		S. Aunet et al.	Real-Time Reconfigurable Subthreshold CMOS Perceptron	**IEEE Transactions on Neural Networks**	Vol. 19, No. 4	Apr. 2008	645 - 657
	PhD	D	1	0		A. Djupdal	Evolving Static Hardware Redundancy for Defect Tolerant FPGAs	Norwegian University of Science and Technology	Trondheim, Norway	25 Apr. 2008	1 - 124
	ieee	D	1	0		S. Aunet	Subthreshold Minority-3 Gates and Inverters Used for 32-bit Serial and Parallel Adders Implemented in 90 nm CMOS	IEEE Norchip International Conference	Trondheim, Norway	16-17 Nov. 2009	5397845 (1-6)
	ieee	D	1	0		A. Dingler et al.	System-Level Energy and Performance Projections for Nanomagnet-based Logic	IEEE/ACM International Symposium on Nanoscale Architectures	San Francisco, CA, USA	30-31 Jul. 2009	21 - 26
	ieee	D	1	0		S. Aunet	On the Reliability of Ultra Low Voltage Circuits Built from Minority-3 Gates	IEEE European Conference on Circuit Theory and Design	Linköping, Sweden	29-31 Aug. 2011	540 - 543
	Journal	**B**	**4**	**4**		A Dingler et al.	Performance and Energy Impact of Locally Controlled NML Circuits	**ACM Journal on Emerging Technologies in Computing Systems**	Vol. 7, No. 1	Jan. 2011	2 (1 - 24)
	ieee	D	1	0		H. Attarzadeh et al.	An ultra-low-power/high-speed 9-bit adder design: Analysis and comparison Vs. technology from 130nm-LP to UTBB FD SOI-28nm	IEEE Nordic Circuits and Systems Conference (NORCAS): NORCHIP & International Symposium on System-on-Chip (SoC)	Oslo, Norway	26 - 28 Oct. 2015	7364365 (1 - 4)
	ieee	D	1	0		A.A. Vatanjou et al.	Energy Efficient Sub/Near-threshold Ripple-carry Adder in Standard 65 nm CMOS	IEEE Asia Symposium on Quality Electronic Design (ASQED)	Kuala Lumpur	4-5 Aug. 2015	7 - 12
	ieee	D	1	0		A.A. Vatanjou et al.	Ultra-Low Voltage Adders in 28 nm FDSOI Exploring Poly-Biasing for Device Sizing	IEEE Nordic Circuits and Systems Conference (NORCAS)	Copenhagen, Denmark	1-2 Nov. 2016	7792895 (1 - 4)
21.00			**21**	**12**	**12.00**						

C109	**ASAP-05**					**V. Beiu, S. Aunet, J. Nyathi, R. Rydberg III, and A. Djupdal**	**On the Advantages of Serial Architectures for Low-Power Reliable Computations**	**IEEE International Conference on Application-specific Systems, Architectures and Processors**	**Samos, Greece**	**23-25 Jul. 2005**	**276 - 281**
	ieee	**D**	**1**	**0**		K. Granhaug and S. Aunet	Improving Yield and Defect Tolerance in Multifunction Subthreshold CMOS Gates	IEEE Symposium on Defect and Fault Tolerance in VLSI Systems	Washington, DC, USA	4-6 Oct. 2006	20 - 28
	IWANN-07	**B**	**4**	**4**		S. Aunet and H.K.O. Berge	Statistical Simulations for Exploring Defect Tolerance and Power Consumption for 4 Subthreshold 1-Bit Addition Circuits	International Work-conference on Artificial Neural Networks (LNCS 4507)	San Sebastian, Spain	20-22 Jun. 2007	455 - 462
	PhD	**D**	**1**	**0**		A. Djupdal	Evolving Static Hardware Redundancy for Defect Tolerant FPGAs	Norwegian University of Science and Technology	Trondheim, Norway	25 Apr. 2008	1 - 124
	Journal	**C**	**2**	**0**		K. Granhaug and S. Aunet	Improving Yield and Defect Tolerance in Subthreshold CMOS Through Output-Wired Redundancy	**Journal of Electronic Testing**	Vol. 24, No. 1-3	Jun. 2008	157 - 163
	PhD	**D**	**1**	**0**		M. He	Contribution à l'étude de l'impact des nanotechnologies sur les architectures : Apprentissage d'inspiration neuronale de	Université de Paris Sud XI	Orsay, France	17 Dec. 2008	1 - 159
	ieee	**D**	**1**	**0**		M.-H. Razmkhah et al.	A Micro-FT-UART for Safety-Critical SoC-Based Applications	IEEE International Conference on Availability, Reliability and Security	Fukuoka, Japan	16-19 Mar. 2009	316 - 321
	PhD	**D**	**1**	**0**		M.R. Scott	Interconnect and Circuit Design for Energy Harvesting Sensors Within a Hybrid CMOS Process using Silicon Nanowires (UMI 3511870)	University of California Davis	Davis, CA, USA	2011	1 - 248
3.67			**11**	**4**	**1.33**						
C110	**IJCNN-05**					**S. Aunet, and V. Beiu**	**Ultra Low Power Fault Tolerant Neural Inspired CMOS Logic**	**IEEE International Joint Conference on Neural Networks**	**Montreal, Canada**	**31 Jul. - 4 Aug. 2005**	**2843 - 2848**
	ifip	**D**	**1**	**0**		S. Aunet and Y. Berg	Three Sub-fJ Power-Delay-Product Subthreshold CMOS Gates	IFIP (International Federation for Information Processing) VLSI-SoC	Perth, Australia	17-19 Oct. 2005	465 - 470
	ieee	**D**	**1**	**0**		K. Granhaug and S. Aunet	Improving Yield and Defect Tolerance in Multifunction Subthreshold CMOS Gates	IEEE Symposium on Defect and Fault Tolerance in VLSI Systems	Washington, DC, USA	4-6 Oct. 2006	20 - 28
	WCCI-06	**A**	**8**	**8**		R. Neville	A Hardware Implementation of Multi-level Threshold Logic for Artificial Neural Net	IEEE World Congress on Computational Intelligence	Vancouver, Canada	16-21 Jul. 2006	2845 - 2851
	VLSID-07	**C**	**2**	**0**		J. Alfredsson et al.	Small Fan-in Floating-Gate Circuits with Application to an Improved Adder Structure	IEEE International Conference on VLSI Design	Bangalore, India	Jan. 2007	314 - 317
	PhD	**D**	**1**	**0**		J. Alfredsson	Limitations of Subthreshold Digital Floating-gate Circuits in Present and Future Nanoscale CMOS Technologies	Mid Sweden University	Sundsvall, Sweden	29 May 2008	1 - 129
	Journal	**A**	**8**	**8**		S. Aunet et al.	Real-Time Reconfigurable Subthreshold CMOS Perceptron	**IEEE Transactions on Neural Networks**	Vol. 19, No. 4	Apr. 2008	645 - 657
	Journal	**C**	**2**	**0**		K. Granhaug and S. Aunet	Improving Yield and Defect Tolerance in Subthreshold CMOS Through Output-Wired Redundancy	**Journal of Electronic Testing**	Vol. 24, No. 1-3	Jun. 2008	157 - 163
	PhD	**D**	**1**	**0**		M. Stanisavljević	On the Dependability of Nanoscale Circuits and Systems: Methodologies and Circuit Architectures	Ecole Polytechnique Federale de Lausanne	Lausanne, Switzerland	27 Mar. 2009	1 - 238
	ieee	**D**	**1**	**0**		M.H. Sulieman	Threshold-Voltage Variations Effects on the Reliability of Nano-scale CMOS Logic Gates	IEEE Nanotechnology Conference	Genoa, Italy	26-30 Jul. 2009	744 - 747
	Book	**B**	**4**	**4**		M. Stanisavljević et al.	Reliability of Nanoscale Circuits and Systems: Methodologies and Circuit Architectures	Springer	New York	2011	1 - 195
29.00			**29**	**20**	**20.00**						
C111	**IJCNN-05**					**V. Beiu, and A. Zawadzki**	**On Kolmogorov's Superpositions: Novel Gates and Circuits for Nanoelectronics?**	**IEEE International Joint Conference on Neural Networks**	**Montreal, Canada**	**31 Jul. - 4 Aug. 2005**	**651 - 656**

	ieee	D	1	0		M. He et al.	Architecture of Neural Synaptic Array, Design and Simulation	IEEE International Conference on Nanotechnology	Hong Kong, China	2-5 Aug. 2007	601 - 604
	Journal	C	2	0		D. Koutsoyiannis et al.	Medium-range Flow Prediction for the Nile: A Comparison of Stochastic and Deterministic Methods	**Hydrological Sciences Journal**	Vol. 53, No. 1	Feb. 2008	142 - 164
	dagstuhl	D	1	0		F. Ablayev and S. Ablayeva	A Communication Complexity Approach to the Superposition Problem	In M. Agrawal et al. (Eds.): "Algebric Methods in Computational Complexity"	Wadern, Germany	11-16 Oct. 2009	1 - 4
	PhD	D	1	0		J. Braun	An Application of Kolmogorov's Superposition Theorem to Function Reconstruction in Higher Dimensions	University of Bonn	Bonn, Germany	Nov. 2009	1 - 185
	Journal	B	4	4		F. Ablayev and S. Ablayeva	A Communication Approach to the Superposition Problem	**Fundamenta Informaticae**	Vol. 104, No. 3	Aug. 2010	185 - 200
9.00			**9**	**4**	**4.00**						

C112	**VLSI-SoC-05**					**S. Aunet, Y. Berg, and V. Beiu**	**Ultra Low-Power Redundant Logic Based on Majority-3 Gates**	**IFIP International Conference on VLSI System-on-Chip**	**Perth, Australia**	**17-19 Oct. 2005**	**553 - 558**
	ieee	D	1	0		K. Granhaug and S. Aunet	Improving Yield and Defect Tolerance in Multifunction Subthreshold CMOS Gates	IEEE Symposium on Defect and Fault Tolerance in VLSI Systems	Washington, DC, USA	4-6 Oct. 2006	20 - 28
	IWANN-07	B	4	4		S. Aunet and H.K.O. Berge	Statistical Simulations for Exploring Defect Tolerance and Power Consumption for 4 Subthreshold 1-Bit Addition Circuits	International Work-conference on Artificial Neural Networks (LNCS 4507)	San Sebastian, Spain	20-22 Jun. 2007	455 - 462
	PhD	D	1	0		M. Stanisavljević	On the Dependability of Nanoscale Circuits and Systems: Methodologies and Circuit Architectures	Ecole Polytechnique Federale de Lausanne	Lausanne, Switzerland	27 Mar. 2009	1 - 238
	Journal	A	8	8		M. Stanisavljević et al.	Optimization of the Averaging Reliability Technique Using Low Redundancy Factors for Nanoscale Technologies	**IEEE Transactions on Nanotechnology**	Vol. 8, No. 3	May 2009	379 - 390
	ieee	D	1	0		S. Aunet	On the Reliability of Ultra Low Voltage Circuits Built from Minority-3 Gates	IEEE European Conference on Circuit Theory and Design	Linköping, Sweden	29-31 Aug. 2011	540 - 543
	ISCAS-11	C	2	0		H.K.O. Berge and S. Aunet	Multi-Objective Optimization of Minority-3 Functions for Ultra-Low Voltage Supplies	IEEE International Symposium on Circuits and Systems	Rio de Janeiro, Brazil	15-18 May 2011	2313 - 2316
	Book	B	4	4		M. Stanisavljević et al.	Reliability of Nanoscale Circuits and Systems: Methodologies and Circuit Architectures	Springer	New York	2011	1 - 195
	ieee	D	1	0		J.E. Bjerkedok et al.	Modular layout-friendly cell library design applied for subthreshold CMOS	IEEE Norchip International Conference	Tampere, Finland	27-28 Oct. 2014	art. 7004747
22.00			**22**	**16**	**16.00**						

C113	**ICM-05**					**V. Beiu**	**The Quest for Practical Redundant Computations**	**IEEE International Conference on Microelectronics**	**Islamabad, Pakistan**	**13-15 Dec. 2005**	**xix**
	acm	D	1	0		H. Jamal	Roadmap to Nanoelectronics for Developing Countries: A Realistic Approach	ACM/WSEAS Int. Conf. on Microelectronics, Nanoelectronics, Optoelectronics	Prague, Czech Republic	12-14 Mar. 2006	36 - 39
	Journal	D	1	0		H. Jamal	Roadmap to Nanoelectronics for Developing Countries: A	**WSEAS Transactions on Electronics**	Vol. 3, No. 4	Apr. 2006	214 - 217
2.00			**2**	**0**	**0.00**						

C115	**AICCSA-06**					**M.H. Sulieman, and V. Beiu**	**Multiplexing Schemes for Single Electron Technologies**	**IEEE International Conference on Computer Systems and Applications**	**Sharjah, UAE**	**8-11 Mar. 2006**	**424 - 428**
	ieee	D	1	0		M.H. Sulieman	Threshold-Voltage Variations Effects on the Reliability of Nano-	IEEE Nanotechnology Conference	Genoa, Italy	26-30 Jul.	744 - 747
	springer	D	1	0		M.H. Sulieman	On the Reliability of Interconnected CMOS Gates Considering	International Conference on Nano-Networks (Springer LNICST	Luzern,	18-20 Oct.	251 - 258
2.00			**2**	**0**	**0.00**						

C117	**DFT-06**					**V. Beiu, W. Ibrahim, Y.A. Alkhawwar, and M.H. Sulieman**	**Gate Failures Effectively Shape Multiplexing**	**IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems**	**Washington, DC, USA**	**2-6 Oct. 2006**	**29 - 37**
	ieee	**D**	**1**	**0**		G.R. Voicu and	Towards Heterogenous 3D-Stacked Reliable Computing with von	IEEE/ACM International Symposium on Nanoscale Architectures	Brooklyn, NY,	Jul. 2013	122 - 127
0.50			**1**	**0**	**0.00**						

C119	**ISMVL-07**					**V. Beiu**	**Grand Challenges of Nanoelectronics and Possible Architectural Solutions**	**IEEE International Symposium on Multiple Valued Logic**	**Oslo, Norway**	**14-16 May 2007**	**a (1 - 7)**
	PhD	**D**	**1**	**0**		C. Gao	Hardware Architectures and Implementations for Associative Memories -- The Building Blocks of Hierarchically Distributed Memories (UMI 3346835)	Portland State University	Portland, OR, USA	2008	1 - 209
	PhD	**D**	**1**	**0**		M. He	Contribution à l'étude de l'impact des nanotechnologies sur les architectures : Apprentissage d'inspiration neuronale de	Université de Paris Sud XI	Orsay, France	17 Dec. 2008	1 - 159
	ieee	**D**	**1**	**0**		D. Hammerstrom and M.S. Zaveri	Prospects for Building Cortex-scale CMOL/CMOS Circuits: A design Space Exploration	IEEE Norchip International Conference	Trondheim, Norway	16-17 Nov. 2009	5397858 (1-8)
	PhD	**D**	**1**	**0**		M. Stanisavljević	On the Dependability of Nanoscale Circuits and Systems: Methodologies and Circuit Architectures	Ecole Polytechnique Federale de Lausanne	Lausanne, Switzerland	27 Mar. 2009	1 - 238
	PhD	**D**	**1**	**0**		M.S. Zaveri	CMOL/CMOS Hardware Architectures and Performance/Price for Bayesian Memory - The Building Block of Intelligent Systems (UMI 3391676)	Portland State University	Portland, OR, USA	29 Oct. 2009	1 - 250
	Chp. 4	**B**	**4**	**4**		D.	CMOL/CMOS Implementations of Bayesian Inference Engine:	In K. Iniewski (ed.): CMOS Processors and Memory	Springer	Jul. 2010	97 - 138
	Journal	**A**	**8**	**8**		M.S. Zaveri and D. Hammerstrom	CMOL/CMOS Implementations of Bayesian Polytree Inference: Digital and Mixed-Signal Architectures and Performance/Price	**IEEE Transactions on Nanotechnology**	Vol. 9, No. 2	Mar. 2010	194 - 211
	PhD	**D**	**1**	**0**		S. Sinha	Nano-scale Studies of the Assembly, Structure and Properties of Hybrid Organic-Silicon Systems	University of Alberta	Edmonton, AL, Canada	Fall 2011	1 - 164
	Book	**B**	**4**	**4**		M. Stanisavljević et al.	Reliability of Nanoscale Circuits and Systems: Methodologies and Circuit Architectures	Springer	New York	2011	1 - 195
	Journal	**A**	**8**	**8**		M.S. Zaveri and D. Hammerstrom	Performance/Price Estimates for Cortex-scale Hardware: A Design Space Exploration	**Neural Networks**	Vol. 24, No. 3	Apr. 2011	291 - 304
30.00			**30**	**24**	**24.00**						

C120	**IWANN-07**					**V. Beiu, W. Ibrahim, and S. Lazarova-Molnar**	**What von Neumann Did Not Say About Multiplexing: Beyond Gates Failures – The Gory Details**	**International Work-Conference on Artificial Neural Networks**	**San Sebastián, Spain**	**19-22 Jun. 2007**	**487 - 496**
	Journal	**A**	**8**	**8**		J. Han et al.	On the Reliability of Computational Structures using Majority Logic	**IEEE Transactions on Nanotechnology**	Vol. 10, No. 5	Sep. 2011	1099 - 1112
	arXiv	**D**	**1**	**0**		B. Cruikshank & K. Jacobs	High-Threshold Low-Overhead Fault-Tolerant Classical Computation and the Replacement of Measurements with	arXiv:1608.08228v1 [quant-ph]		29 Aug. 2016	1 - 5
9.00			**9**	**8**	**8.00**						

C122	**CSCC-07**					**S. Lazarova-Molnar, V. Beiu, and W. Ibrahim**	**A Strategy for Reliability Assessment of Future Nano-Circuits**	**WSEAS International Conference on Circuits, Systems, Communications, Computers**	**Agios Nikolaos, Crete, Greece**	**23-28 Jul. 2007**	**60 - 65**
	PhD	**D**	**1**	**0**		M. Stanisavljević	On the Dependability of Nanoscale Circuits and Systems: Methodologies and Circuit Architectures	Ecole Polytechnique Federale de Lausanne	Lausanne, Switzerland	27 Mar. 2009	1 - 238
	PhD	**D**	**1**	**0**		K. Lingasubramanian	Probabilistic Error Analysis Models for Nano-Domain VLSI Circuits (UMI 3424479)	University of South Florida	Tampa, FL, USA	3 Mar. 2010	1 - 114
	Journal	**B**	**4**	**4**		K. Lingasubramanian et al.	Maximum Error Modeling for Fault-tolerant Computation using Maximum a posteriori (MAP) Hypothesis	**Microelectronics Reliability**	Vol. 51, No. 2	Feb. 2011	485 - 501
	Book	**B**	**4**	**4**		M. Stanisavljević et al.	Reliability of Nanoscale Circuits and Systems: Methodologies and Circuit Architectures	Springer	New York	2011	1 - 195
10.00			**10**	**8**	**8.00**						
C123	**IEEE-NANO-07**					**V. Beiu, W. Ibrahim, and S. Lazarova-Molnar**	**A Fresh Look at Majority Multiplexing – When Devices Get Into the Picture**	**IEEE International Conference on Nanotechnology**	**Hong Kong, China**	**2-5 Aug. 2007**	**883 - 888**
	PhD	**D**	**1**	**0**		M. Stanisavljević	On the Dependability of Nanoscale Circuits and Systems: Methodologies and Circuit Architectures	Ecole Polytechnique Federale de Lausanne	Lausanne, Switzerland	27 Mar. 2009	1 - 238
	Journal	**A**	**8**	**8**		M. Stanisavljević et al.	Optimization of the Averaging Reliability Technique Using Low Redundancy Factors for Nanoscale Technologies	**IEEE Transactions on Nanotechnology**	Vol. 8, No. 3	May 2009	379 - 390
	ieee	**D**	**1**	**0**		M. Stanisavljević et al.	Optimization of Nanoelectronic Systems Reliability Under Massive Defect Density Using Distributed R-fold Modular Redundancy (DRMR)	IEEE International Symposium on defect and Fault Tolerance in VLSI Systems	Chicago, IL, USA	7-9 Oct. 2009	340 - 348
	springer	**D**	**1**	**0**		M. Stanisavljević et al.	Optimization of Nanoelectronic Systems Reliability by Reducing Logic Depth	International Conference on Nano-Networks (Springer LNICST 20)	Luzern, Switzerland	18-20 Oct. 2009	70 - 75
	Book	**B**	**4**	**4**		M. Stanisavljević et al.	Reliability of Nanoscale Circuits and Systems: Methodologies and Circuit Architectures	Springer	New York	2011	1 - 195
	Chp. 18	**A**	**8**	**8**		M. Stanisavljević et al.	Reliability of Nanoelectrinic VLSI	In K. Iniewski (ed.): Advanced Circuits for Emerging Technologies	John Wiley	May 2012	463 - 482
	PhD	**D**	**1**	**0**		N. Aymerich	Variability-aware Architectures based on Hardware Redundancy for Nanoscale Reliable Computation	Universidad Politecnica de Catalunya	Barcelona, Spain	Dec. 2013	1 - 149
24.00			**24**	**20**	**20.00**						
C124	**IEEE-NANO-07**					**R.M. Beiu, C.D. Stanescu, and V. Beiu**	**Highly Sensitive Nano-Photonic Embedded Sensors**	**IEEE International Conference on Nanotechnology**	**Hong Kong, China**	**2-5 Aug. 2007**	**737 - 741**
	Journal	**C**	**2**	**0**		R.M. Beiu, C.D. Stanescu, and A. Carstoiu	On 3D photonic crystals a brief evaluation of their main characteristics for various topologies	**UPB Scientific Bulletin, Series C: Electrical Engineering**	Vol. 70, No. 2	2008	41 - 52
2.00			**2**	**0**	**0.00**						

C127	**IIT-07**					**W. Ibrahim, V. Beiu, and Y.A. Alkhawwar**	**On the Reliability of Four Full Adder Cells**	**IEEE International Conference Innovations in Information Technology**	**Dubai, UAE**	**18-20 Nov. 2007**	**720 - 724**
	PhD	**D**	**1**	**0**		M. Stanisavljević	On the Dependability of Nanoscale Circuits and Systems: Methodologies and Circuit Architectures	Ecole Polytechnique Federale de Lausanne	Lausanne, Switzerland	27 Mar. 2009	1 - 238
	Book	**B**	**4**	**4**		M. Stanisavljević et al.	Reliability of Nanoscale Circuits and Systems: Methodologies and Circuit Architectures	Springer	New York	2011	1 - 195
	Chp. 18	**A**	**8**	**8**		M. Stanisavljević et al.	Reliability of Nanoelectrinic VLSI	In K. Iniewski (ed.): Advanced Circuits for Emerging Technologies	John Wiley	May 2012	463 - 482
13.00			**13**	**12**	**12.00**						

C130	**ICSPC-07**					**S. Lazarova-Molnar, V. Beiu, and W. Ibrahim**	**Reliability – The Fourth Optimization Pillar of Nanoelectronics**	**IEEE International Conference on Signal Processing and Communications**	**Dubai, UAE**	**24-27 Nov. 2007**	**73 - 76**
	PhD	**D**	**1**	**0**		M. Stanisavljević	On the Dependability of Nanoscale Circuits and Systems: Methodologies and Circuit Architectures	Ecole Polytechnique Federale de Lausanne	Lausanne, Switzerland	27 Mar. 2009	1 - 238
	Book	**B**	**4**	**4**		M. Stanisavljević et al.	Reliability of Nanoscale Circuits and Systems: Methodologies and Circuit Architectures	Springer	New York	2011	1 - 195
5.00			**5**	**4**	**4.00**						

C133	**ISCAS-08**					**V. Beiu, and W. Ibrahim**	**Does the Brain Really Outperform Rent's Rule?**	**IEEE International Symposium on Circuits and Systems**	**Seattle, WA, USA**	**18-21 May 2008**	**640 - 643**
	ESANN-09	**B**	**4**	**4**		J. Partzsch and R. Schuffny	On the Routing Complexity of Neural Network Models -- Rent's Rule Revisited	European Symposium on Artificial Neural Networks	Bruges, Belgium	22-24 Apr. 2009	595 - 600
	PhD	**D**	**1**	**0**		M.S. Zaveri	CMOL/CMOS Hardware Architectures and Performance/Price for Bayesian Memory - The Building Block of Intelligent Systems (UMI 3391676)	Portland State University	Portland, OR, USA	29 Oct. 2009	1 - 250
	Journal	**A**	**8**	**8**		D.S. Bassett et al.	Efficient Physical Embedding of Topologically Complex Information Processing Networks in Brains and Computer Circuits	**PLoS Computational Biology**	Vol. 6, No. 4	Apr. 2010	e1000748 (1-14)
	Journal	**A**	**8**	**8**		L.C. Gouveia et al.	An Asynchronous Spike Event Coding Scheme for Programmable Analog Arrays	**IEEE Transactions on Circuits and Systems I**	Vol. 58, No. 4	Apr. 2011	791 - 799
	Journal	**A**	**8**	**8**		J. Partzsch and R. Schuffny	Analyzing the Scaling of Connectivity in Neuromorphic Hardware and in Models of Neural Networks	**IEEE Transactions on Neural Networks**	Vol. 22, No. 6	Jun. 2011	919 - 935
	Journal	**A**	**8**	**8**		P. Ruch et al.	Toward Five-Dimensional Scaling: How Density Improves Efficiency in Future Computers	**IBM Journal of Research and Development**	Vol. 55, No. 5	Sept.-Oct. 2011	15 (1-13)
	Journal	**A**	**8**	**8**		M.S. Zaveri and D. Hammerstrom	Performance/Price Estimates for Cortex-scale Hardware: A Design Space Exploration	**Neural Networks**	Vol. 24, No. 3	Apr. 2011	291 - 304
	Journal	**A**	**8**	**8**		G. Vernizzi et al.	Topological Constraints for E. F. Rent's Work on Microminiature Packaging and Circuitry	**IBM Journal of Research and Development**	Vol. 58, No. 2	Apr. 2014	13 : 1 - 17
	ProQuest	**D**	**1**	**0**		B.J. West	A Fractional Probability Calculus View of Allometry	**Systems**	Vol. 2, No. 2	Apr. 2014	89 - 118
	Journal	**C**	**2**	**0**		W. Li et al.	A Basic Chemical Synaptic Euler Model and Its Triad Trigger Topology	**Chinese Journal of Electronics**	Vol. 25	Jul. 2016	1 - 6

	oxford	D	1	0		M.M. Sperry et al.	Rentian Scaling for the Measurement of Optimal Embedding of Complex Networks into Physical Space	**Journal of Complex Networks**	Advanced access	3 Aug. 2016	1 - 20
57.00			57	52	52.00						
C134	**NANOARCH-08**					**B.A.M. Madappuram, V. Beiu, P.M. Kelly, and L.J. McDaid**	**On Brain-inspired Connectivity and Hybrid Network Topologies**	**IEEE/ACM International Symposium on Nanoscale Architectures**	**Anaheim, CA, USA**	**8-13 Jun. 2008**	**54 - 61**
	ieee	D	1	0		D. Hammerstrom and M.S. Zaveri	Prospects for Building Cortex-scale CMOL/CMOS Circuits: A design Space Exploration	IEEE Norchip International Conference	Trondheim, Norway	16-17 Nov. 2009	5397858 (1-8)
	PhD	D	1	0		M.S. Zaveri	CMOL/CMOS Hardware Architectures and Performance/Price for Bayesian Memory - The Building Block of Intelligent Systems (UMI 3391676)	Portland State University	Portland, OR, USA	29 Oct. 2009	1 - 250
	ISCAS-10	C	2	0		Z. Chiragwandi et al.	Robustness of Logic Gates and Reconfigurability of Neuromorphic Switching Networks	IEEE International Symposium on Circuits and Systems	Paris, France	30 May - 2 Jun. 2010	1671 - 1674
	PhD	D	1	0		J. Sköldberg	Molecular Electronics – Modeling, Devices and Architecture	Department of Microtechnology and Nanoscience, Chalmers University of Technology	Goteborg, Sweden	24 Sept. 2010	1 - 137
	Journal	A	8	8		G. Snider at al.	From Synapses to Circuitry: Using Memristive Memory to Explore the Electronic Brain	**Computer**	Vol. 44, No. 2	Feb. 2011	21 - 28
	Journal	A	8	8		M.S. Zaveri and D. Hammerstrom	Performance/Price Estimates for Cortex-scale Hardware: A Design Space Exploration	**Neural Networks**	Vol. 24, No. 3	Apr. 2011	291 - 304
	Journal	A	8	8		G. Vernizzi et al.	Topological Constraints for E. F. Rent's Work on Microminiature Packaging and Circuitry	**IBM Journal of Research and Development**	Vol. 58, No. 2	Apr. 2014	13 : 1 - 17
14.50			29	24	12.00						
C135	**M&S–MTSA-08**					**S. Lazarova-Molnar, and V. Beiu**	**Reliability Modeling of Circuits with Multi-State Aging Gates**	**Modeling & Simulation – Methodology, Tools, Software Applications**	**Edinburgh, UK**	**16-19 Jun. 2008**	**43 - 47**
	ieee	D	1	0		A. Beg	A Composition-Aware Model for Unreliable Circuits	IEEE International Midwest Symposium on Circuit and Systems	Seattle, WA, USA	1-4 Aug. 2010	853 - 856
1.00			1	0	0.00						
C137	**IC-SAMOS-08**					**V. Beiu, B.A.M. Madappuram, and M. McGinnity**	**On Brain-inspired Hybrid Topologies for Nano-architectures — A Rent's Rule Approach**	**IEEE International Conference on Embedded Computer Systems**	**Samos, Greece**	**21-24 Jul. 2008**	**33 - 40**
	Journal	C	2	0		L. Wang et al.	GNLS: A Hybrid On-Chip Communication Architecture for SoC Designs	**International Journal of High Performance Systems Architecture**	Vol. 3, No. 2-3	May 2011	157 - 166
	Journal	A	8	8		G. Vernizzi et al.	Topological Constraints for E. F. Rent's Work on Microminiature Packaging and Circuitry	**IBM Journal of Research and Development**	Vol. 58, No. 2	Apr. 2014	13 : 1 - 17
10.00			10	8	8.00						
C138	**IPGC-08**					**R.M. Beiu, and V. Beiu**	**Fiber Optic Mechanical Sensor Based on a Triangular-lattice Photonic Crystal**	**IEEE International Photonics Global Conference**	**Singapore**	**8-11 Dec. 2008**	**4781347 (1 - 4)**

	Journal	**A**	**8**	**8**		Y. Zhao et al.	Research Advances of Photonic Crystal Gas and Liquid sensors	**Sensors and Actuators B: Chemical**	Vol. 160, No. 1	15 Dec. 2011	1288 - 1297
	Chp. 6	**B**	**4**	**4**		G. Korotcenkov	Photonic Crystals	**Handbook of Gas Sensor Materials**	Springer	2014	111 - 119
	Journal	**B**	**4**	**4**		Y. Wang et al.	A Super Narrow Band Filter Based on Silicon 2D Photonic Crystal Resonator and Reflectors	**Optics Communications**	Vol. 363	15 Mar. 2016	13 - 20
16.00			**16**	**16**	**16.00**						

C142	**DSN-09**					**V. Beiu, and W. Ibrahim**	**On CMOS Circuit Reliability from the MOSFETs and the Input Vectors**	**IEEE/IFIP International Conference on Dependable Systems and Networks**	**Estoril, Lisbon, Portugal**	**29 Jun. - 2 Jul. 2009**	
	Journal	**A**	**8**	**8**		J. Han et al.	On the Reliability of Computational Structures using Majority Logic	**IEEE Transactions on Nanotechnology**	Vol. 10, No. 5	Sep. 2011	1099 - 1112
8.00			**8**	**8**	**8.00**						

C144	**IEEE-NANO-09**					**W. Ibrahim, V. Beiu, and H. Amer**	**How Much Input Vectors Affect Nano-Circuit's Reliability Estimates**	**IEEE International Conference on Nanotechnology**	**Genoa, Italy**	**26-30 Jul. 2009**	**699 - 702**
	Journal	**A**	**8**	**8**		J. Han et al.	On the Reliability of Computational Structures using Majority Logic	**IEEE Transactions on Nanotechnology**	Vol. 10, No. 5	Sep. 2011	1099 - 1112
	ieee	**D**	**1**	**0**		U. Khalid et al.	Improvement in Reliability by Changing the Deterministic Inputs of Nanoscale Circuits	IEEE Regional Symposium on Micro and Nanoelectronics	Kota Kinabalu, Sabah, Malaysia	28-30 Sept. 2011	195 - 197
	Journal	**A**	**8**	**8**		W. Ibrahim et al.	Accurate and Efficient Estimation of Logic Circuits Reliability Bounds	**IEEE Transactions on Computers**	Vol. 64, No. 5	May 2015	1217 - 1229
	Journal	**A**	**8**	**8**		W. Ibrahim	Identifying the Worst Reliability Input Vectors and the Associated Critical Logic Gates	**IEEE Transactions on Computers**	Vol. 65, No. 6	Jul. 2016	1748 - 1760
	SCSC-16	**B**	**4**	**4**		W. Ibrahim and H. Amer	Critical nodes count algorithm for accurate input vectors reliability ranking	International Summer Computer Simulation Conference	Montreal, Quebec, Canada	24-27 Jul. 2016	art. 19 (http://dl.acm.org/citation.cfm?id=3015593)
	ieee	**D**	**1**	**0**		B. Yang et al.	An Approach for Digital Circuit Error/Reliability Propagation Analysis Based on Conditional Probability	IEEE Irish Signals and Systems Conference (ISSC)	Londonderry, UK	21-22 Jun. 2016	1 - 6
30.00			**30**	**28**	**28.00**						

C145	**IEEE-NANO-09**					**V. Beiu, B.A.M. Madappuram, P.M. Kelly, and L.J. McDaid**	**On Brain-inspired Hierarchical Network Topologies**	**IEEE International Conference on Nanotechnology**	**Genoa, Italy**	**26-30 Jul. 2009**	**202 - 205**
	Journal	**A**	**8**	**8**		G. Vernizzi et al.	Topological Constraints for E. F. Rent's Work on Microminiature Packaging and Circuitry	**IBM Journal of Research and Development**	Vol. 58, No. 2	Apr. 2014	13 : 1 - 17
4.00			**8**	**8**	**4.00**						

C146	**Nano-Net-09**					**W. Ibrahim, and V. Beiu**	**A Bayesian-based EDA Tool for Nano-Circuits Reliability Calculations**	**International ICST Conference on Nano-Networks**	**Luzern, Switzerland**	**18-20 Oct. 2009**	**276 - 284**
	springer	**D**	**1**	**0**		A. Beg	Improving Nano-Circuit Reliability Estimates by Using Neural Methods	ICST International Conference on Nano-Networks (LNICS)	Luzern, Switzerland	18-20 Oct. 2009	270 - 275
	CiteSeerX	**D**	**1**	**0**		M.H. Chamansara et al.	High Performance and Low-Power Full Adder	**International Journal of Emerging Science and Engineering**	Vol. 2, No. 1	Nov. 2013	5 - 8

	acm	D	1	0		W. Ibrahim	Accurate and Effective Algorithm for Estimating the Reliability of Digital Combinational Circuits	ACM Annual Simulation Symposium (Spring Simulation Multi-Conference SpringSim'13)	San Diego, CA, USA	Apr. 2013	65 - 72
	Journal	C	2	0		J. Xiao et al.	A Method of Circuit Reliability Estimation Based on Iterative PTM Model	**Chinese Journal of Computers**	Vol. 37, No. 7	Jul. 2014	1508 - 1520
	SCSC-16	B	4	4		W. Ibrahim and H. Amer	Critical nodes count algorithm for accurate input vectors reliability ranking	International Summer Computer Simulation Conference	Montreal, Quebec, Canada	24-27 Jul. 2016	art. 19 (http://dl.acm.org/citation.cfm?id=3015593)
9.00			**9**	**4**	**4.00**						

C147	**Nano-Net-09**					**V. Beiu, W. Ibrahim, and R.Z. Makki**	**On Wires Holding a Handful of Electrons**	**International ICST Conference on Nano-Networks**	**Luzern, Switzerland**	**18-20 Oct. 2009**	**259 - 269**
	springer	D	1	0		M.H. Sulieman	On the Reliability of Interconnected CMOS Gates Considering MOSFET Threshold-Voltage Variations	International Conference on Nano-Networks (Springer LNICST 20)	Luzern, Switzerland	18-20 Oct. 2009	251 - 258
1.00			**1**	**0**	**0.00**						

C150	**IIT-09**					**W. Ibrahim, and V. Beiu**	**Reliability of NAND-2 CMOS Gates from Threshold Voltage Variations**	**IEEE International Conference Innovations in Information Technology**	**Al Ain, UAE**	**15-17 Dec. 2009**	**135 - 139**
	ieee	D	1	0		H. Chen et al.	A Transistor-Level Stochastic Approach for Evaluating the Reliabiltiy of Digital Nanometric CMOS Circuits	IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems	Vancouver, Canada	3-5 Oct. 2011	60 - 67
	ieee	D	1	0		M.H. Sulieman and W. Ibrahim	Design of Low-Power and Reliable Nano Adders	IEEE International Conference on Nanotechnology	Portland, OR, USA	15-18 Aug. 2011	441 - 444
	ProQuest	D	1	0		A. Beg et al.	Effect of Channel Lengthening and Threshold Voltage Variation on a Nanometric Gate's Delay and Power	WorldComp'12 / CDES-12	Las Vegas, NV, USA	16-19 Jul. 2012	55 - 62
	ieee	D	1	0		T. Ban et al.	Modeling of Transient Faults and Fault-tolerant Design in Nanoelectronics	IEEE International Midwest Symposium on Circuits and Systems	Columbus, OH, USA	Aug. 2013	545 - 548
	acm	D	1	0		A. Antoniadis et al.	Energy-Efficient Circuit Design	ACM Innovations in Theoretical Computer Science (ITCS)	Princeton, NJ, USA	Jan. 2014	1 - 9
5.00			**5**	**0**	**0.00**						

C151	**ICWN'10**					**L. Zhang, H. Elsayed, and V. Beiu**	**A Position-Based Broadcast Relay Approach in Mobile Vehicle-to-Vehicle Network**	**International Conference on Wireless Networks (part of WorldComp'10)**	**Las Vegas, NV, USA**	**12-15 Jul. 2010**	**611 - 616**
	CiteSeerX	D	1	0		S. Sharma et al.	An Intersection based Traffic Monitoring using VANET	**International Journal of Computer Applications**	Vol. 117, No. 11	May 2015	25 - 30
1.00			**1**	**0**	**0.00**						

C152	**IEEE-NANO-10**					**M.H. Sulieman, V. Beiu, and W. Ibrahim**	**Low-Power and Highly Reliable Logic Gates: Transistor-level Optimizations**	**IEEE International Conference on Nanotechnology**	**Seoul, Korea**	**17-20 Aug. 2010**	**254 - 257**
	ieee	D	1	0		M.H. Sulieman and W. Ibrahim	Design of Low-Power and Reliable Nano Adders	IEEE International Conference on Nanotechnology	Portland, OR, USA	15-18 Aug. 2011	441 - 444
	ProQuest	D	1	0		A. Beg et al.	Effect of Channel Lengthening and Threshold Voltage Variation on a Nanometric Gate's Delay and Power	WorldComp'12 / CDES-12	Las Vegas, NV, USA	16-19 Jul. 2012	55 - 62
	CiteSeerX	D	1	0		M.H. Chamansara et al.	High Performance and Low-Power Full Adder	**International Journal of Emerging Science and Engineering**	Vol. 2, No. 1	Nov. 2013	5 - 8

	elsevier	D	1	0		T.C. Cavalcante et al.	The Design of Reliable Circuits Using Logic Redundancy	International Conference in Through-life Engineering Services	Vol. 22	2014	138 - 141
	Journal	B	4	4		R. Lorenzo and S. Chaudhury	Dynamic Threshold Sleep Transistor Technique for High Speed and Low Leakage in CMOS Circuits	**Circuits, Systems, and Signal Processing**	In press	24 Oct. 2016	1 - 18
8.00			8	4	4.00						

C156	**NEWCAS-11**					**A. Beg, V. Beiu, and W. Ibrahim**	**Atto Joule CMOS Gates Using Reversed Sizing and W/L Swapping**	**IEEE International New Circuits and Systems Conference**	**Bordeaux, France**	**26-29 Jun. 2011**	**498 - 501**
	ProQuest	D	1	0		A. Beg et al.	Effect of Channel Lengthening and Threshold Voltage Variation on a Nanometric Gate's Delay and Power	WorldComp'12 / CDES-12	Las Vegas, NV, USA	16-19 Jul. 2012	55 - 62
	Journal	C	2	0		A. Beg	A Web-based Method for Building and Simulating Standard Cell Circuits — A Classroom Application	**Computer Applications in Engineering Education**	Vol. 23, No. 2	Mar. 2015	304 - 313
	FIT-14	C	2	0		A. Beg	Automating the CMOS Gate Sizing for Reduced Power/Energy	IEEE International Conference on Frontiers of Information Technology (FIT)	Islamabad, Pakistan	16-19 Dec. 2014	193 - 196
5.00			5	0	0.00						

C157	**IJCNN-11**					**J.J. Wade, L.J. McDaid, J. Harkin, V. Crunelli, J.A.S. Kelso, and V. Beiu**	**Exploring Retrograde Signaling via Astrocytes as a Mechanism for Self Repair**	**IEEE International Joint Conference on Neural Networks**	**San Jose, CA, USA**	**31 Jul. - 5 Aug. 2011**	**3149 - 3155**
	Journal	A	8	8		J.J. Wade et al.	Bidirectional Coupling between Astrocytes and Neurons Mediates Learning and Dynamic Coordination in the Brain: A Multiple Modeling Approach	**PLoS ONE**	Vol. 6, No. 12	Dec. 2011	e29445 (1 - 24)
	Journal	A	8	8		J.A.S. Kelso et al.	Outline of a General Theory of Behavior and Brain Coordination	**Neural Networks**	Vol. 37	Jan. 2013	120 - 131
	ebscohost	D	1	0		J. Wade et al.	Self-repair in a Bidirectionally Coupled Astrocyte-Neuron (AN) System Based on Retrograde Signaling	**Frontiets in Computational Neuroscience (ISI IF = 2.653)**	Vol. 6	Sept. 2012	76 (1 - 12)
	Journal	A	8	8		J.A.S. Kelso et al.	Outline of a General Theory of Behavior and Brain Coordination	**Neural Networks**	Vol. 37, No. 1	Jan. 2013	120 - 131
	Journal	A	8	8		M. Naeem et al.	On the Role of Astroglial Syncytia in Self-Repairing Spiking Neural Networks	**IEEE Transactions on Neural Networks and Learning Systems**	Vol. 26, No. 10	Oct. 2015	2370 - 2380
	Journal	A	8	8		J. Liu et al.	Scalable Networks-on-Chip Interconnected Architecture for Astrocyte-Neuron Networks	**IEEE Transactions on Circuits and Systems I**	Vol. 63, No. 12	Dec. 2016	2290 - 2303
10.25			41	40	10.00						

C159	**IEEE-NANO-11**					**W. Ibrahim, A. Beg, and V. Beiu**	**Highly Reliable and Low-Power Full Adder Cell**	**IEEE International Conference on Nanotechnology**	**Portland, OR, USA**	**15-18 Aug. 2011**	**500 - 503**
	ieee	D	1	0		R. Johri et al.	Comparative Analysis of 10T and 14T Full Adder at 45nm Technology	IEEE International Conference on Parallel Distributed and Grid Computing	Waknaghat, India	6-8 Dec. 2012	833 - 837
	ieee	D	1	0		A.K. Shrivastava and S. Akashe	Design High Performance and Low Power 10T Full Adder Cell Using Double Gate MOSFET at 45nm Technology	IEEE International Conference on Control Computing Communication & Materials (ICCCCM)	Allahabad, Pakistan	Aug. 2013	1 - 5
	FIT-14	C	2	0		A. Beg	Automating the CMOS Gate Sizing for Reduced Power/Energy	IEEE International Conference on Frontiers of Information Technology (FIT)	Islamabad, Pakistan	16-19 Dec. 2014	193 - 196

	SMC-14	B	4	4		A. Beg	Designing Array-based CMOS Logic Gates by Using a Feedback Control System	IEEE International Conference on Systems, Man and Cybernetics (SMC)	San Diego, CA, USA	5-8 Oct. 2014	935 - 939
	Journal	B	4	4		A. Beg	Automating the sizing of transistors in CMOS gates for low-power and high-noise margin operation	**International Journal of Circuit Theory and Applications**	Vol. 43, No. 11	Nov. 2015	1637 - 1654
	Journal	C	2	0		M Bahadori et al.	A Comparative Study on Performance and Reliability of 32-bit Binary Adders	**Integration, the VLSI Journal**	Vol. 53	Mar. 2016	54 - 67
14.00			**14**	**8**	**8.00**						

C161	**IEEE-NANO-11**					**V. Beiu, A. Beg, and W. Ibrahim**	**Atto-Joule Gates for the Whole Voltage Range**	**IEEE International Conference on Nanotechnology**	**Portland, OR, USA**	**15-18 Aug. 2011**	**1424 - 1429**
	SMC-14	B	4	4		A. Beg	Designing Array-based CMOS Logic Gates by Using a Feedback Control System	IEEE International Conference on Systems, Man and Cybernetics (SMC)	San Diego, CA, USA	5-8 Oct. 2014	935 - 939
	Journal	B	4	4		A. Beg	Automating the sizing of transistors in CMOS gates for low-power and high-noise margin operation	**International Journal of Circuit Theory and Applications**	Vol. 43, No. 11	Nov. 2015	1637 - 1654
8.00			**8**	**8**	**8.00**						

C163	**IEEE-NANO-12**					**V. Beiu, A. Beg, W. Ibrahim, and F. Kharbash**	**Towards Ultra-Low Voltage/Power Using Unconventionally Sized Arrays of Transistors**	**IEEE International Conference on Nanotechnology**	**Birmingham, UK**	**20-23 Aug. 2012**	**6322071 (1 - 5)**
	SMC-14	B	4	4		A. Beg	Designing Array-based CMOS Logic Gates by Using a Feedback Control System	IEEE International Conference on Systems, Man and Cybernetics (SMC)	San Diego, CA, USA	5-8 Oct. 2014	935 - 939
	Journal	B	4	4		A. Beg	Automating the sizing of transistors in CMOS gates for low-power and high-noise margin operation	**International Journal of Circuit Theory and Applications**	Vol. 43, No. 11	Nov. 2015	1637 - 1654
4.00			**8**	**8**	**4.00**						

C164	**ICNAAM-12**					**V. Beiu, M. Calame, G. Cuniberti, C. Gamrat, Z. Konkoli, D. Vuillaume, G. Wendin, and S. Yitzchaik**	**Aspects of Computing with Locally Connected Networks**	**AIP International Conference on Numerical Analysis and Applied Mathematics**	**Kos, Greece**	**19-25 Sept. 2012**	**1875 - 1879**
	arXiv	D	1	0		Z. Konkoli and G. Wendin	Toward Bio-inspired Information Processing with Networks of Nano-scale Switching Elements	arXiv:1311.6259v1 [cs.ET]		Nov. 2013	1 - 34
	e-mrs	D	1	0		Z. Konkoli and G. Wendin	Bio-inspired information processing with memristor switching networks	European Materials Research Society Spring Meeting (E-MRS)	Lille, France	May 2014	http://www.european-mrs.com/meetings/archives/2014/2014-spring
	Journal	C	2	0		Z. Konkoli and G. Wendin	On Information Processing with Networks of Nano-Scale Switching Elements	**International Journal of Unconventional Computing**	Vol. 10, No. 5-6	Jun. 2014	405 - 428
	Journal	A	8	8		J. Liao et al.	Ordered Nanoparticle Arrays Interconnected by Molecular Linkers: Electronic and Optoelectronic Properties	**Chemical Society Reviews**	Vol. 44, No. 4	4 Nov. 2015	999 - 1-14
	Journal	A	8	8		Y. Viero et al.	High Conductance Ratio in Molecular Optical Switching of Functionalized Nanoparticle Self-Assembled Nanodevices	**The Journal of Physical Chemistry C**	Vol. 119, No. 36	Aug. 2015	21173 - 21183

3.33			**20**	**16**	**2.67**						
C165	**CAS-12**					**A. Beg, V. Beiu, and W. Ibrahim**	**Unconventional Transistor Sizing for Reducing Power Alleviates Threshold Voltage Variations**	**IEEE International Semiconductor Conference**	**Sinaia, Romania**	**15-17 Oct. 2012**	**429 - 432**
	CSCWD-13	**B**	**4**	**4**		A. Beg et al.	A Collaborative Platform for Facilitating Standard Cell Characterization	IEEE International Conference on Computer Supported Cooperative Work in Design	Whistler, BC, Canada	Jun. 2013	202 - 206
	Journal	**C**	**2**	**0**		A. Beg	A Web-based Method for Building and Simulating Standard Cell Circuits — A Classroom Application	**Computer Applications in Engineering Education**	Vol. 23, No. 2	Mar. 2015	304 - 313
	FIT-14	**C**	**2**	**0**		A. Beg	Automating the CMOS Gate Sizing for Reduced Power/Energy	IEEE International Conference on Frontiers of Information Technology (FIT)	Islamabad, Pakistan	16-19 Dec. 2014	193 - 196
	SMC-14	**B**	**4**	**4**		A. Beg	Designing Array-based CMOS Logic Gates by Using a Feedback Control System	IEEE International Conference on Systems, Man and Cybernetics (SMC)	San Diego, CA, USA	5-8 Oct. 2014	935 - 939
	europment	**D**	**1**	**0**		A. Beg and A. Beg	Investigating the Reliability of Nano-Scaled BDD-Based Gates	International Conference on Circuits, Systems, Signal Processing, Communications and Computers (CSCC)	Venice, Italy	Mar. 2014	84 - 89
	ProQuest	**D**	**1**	**0**		A. Beg and A. Beg	Reliability of Nano-Scaled Logic Gates Based on Binary Decision Diagrams	International Conference on Modeling, Simulation and Visualization Methods (MSV), part of WORLDCOMP'14	Las Vegas, NV, USA	Jul. 2014	1 - 7
14.00			**14**	**8**	**8.00**						
C166	**CAS-12**					**V. Beiu, L. Iordaconiu, A. Beg, W. Ibrahim, and F. Kharbash**	**Low Power and Highly Reliable Gates Using Arrays of Optimally Sized Transistors**	**IEEE International Semiconductor Conference**	**Sinaia, Romania**	**15-17 Oct. 2012**	**433 - 436**
	PhD	**D**	**1**	**0**		H.K.O. Berge	Improvements towards Optimal Design of Reliable Subthreshold Digital CMOS with applications in Logic and Memory	Faculty of Mathematics and Natural Sciences, University of Oslo (No. 1658)	Oslo, Norway	15 Jul. 2015	1 - 111
0.33			**1**	**0**	**0.00**						
C169	**ISQED-13**					**V. Beiu, A. Beg, W. Ibrahim, F. Kharbash, and M. Alioto**	**Enabling Sizing for Enhancing the Static Noise Margins**	**IEEE International Symposium on Quality in Electronic Design**	**Santa Clara, CA, USA**	**4-6 Mar. 2013**	**278 - 285**
	ieee	**D**	**1**	**0**		A. Beg and A. Elchouemi	Enhancing Static Noise Margin while Reducing Power Consumption	IEEE International Midwest Symposium on Circuits and Systems	Columbus, OH, USA	Aug. 2013	348 - 351
	FIT-14	**C**	**2**	**0**		A. Beg	Automating the CMOS Gate Sizing for Reduced Power/Energy	IEEE International Conference on Frontiers of Information Technology (FIT)	Islamabad, Pakistan	16-19 Dec. 2014	193 - 196
	SMC-14	**B**	**4**	**4**		A. Beg	Designing Array-based CMOS Logic Gates by Using a Feedback Control System	IEEE International Conference on Systems, Man and Cybernetics (SMC)	San Diego, CA, USA	5-8 Oct. 2014	935 - 939
	Journal	**B**	**4**	**4**		A. Beg	Automating the sizing of transistors in CMOS gates for low-power and high-noise margin operation	**International Journal of Circuit Theory and Applications**	Vol. 43, No. 11	Nov. 2015	1637 - 1654
3.67			**11**	**8**	**2.67**						
C171	**GCC-13**					**N.V. Acharya, J.L. Raju, A. Kumar, M. Tache, and V. Beiu**	**Monte Carlo Analysis of the Static Noise Margins for CMOS Gates in Predictive Technology Models**	**IEEE GCC Conference and Exhibition**	**Doha, Qatar**	**17-20 Nov. 2013**	**5 - 10**

	Journal	**C**	**2**	**0**		J. Xiao et al.	Circuit Reliability Estimation Based on an Iterative PTM Model with Hybrid Coding	**Microelectronics Journal**	Vol. 52	Jun. 2016	117 - 123
0.67			**2**	**0**	**0.00**						
C176	**IEEE-NANO-14**					**V. Beiu, and L. Daus**	**Review of Reliability Bounds for Consecutive-k-out-of-n Systems**	**IEEE International Conference on Nanotechnology**	**Toronto, ON, Canada**	**18-21 Aug. 2014**	**302 - 307**
	Journal	**A**	**8**	**8**		E. Chiodo and D. Lauria	Some Basic Properties of the Failure Rate of Redundant Reliability Systems in Industrial Electronics Applications	**IEEE Transactions on Industrial Electronics**	Vol. 62, No. 8	Aug. 2015	5055 - 5062
	arXiv	**D**	**1**	**0**		S. Cowell	A Formula for the Reliability of a d-dimensional Consecutive-k-out-of-n:F System	**International Journal of Combinatorics**	Vol. 2015	2015	140909 (1 - 5)
9.00			**9**	**8**	**8.00**						
C177	**IEEE-NANO-14**					**V. Beiu, W. Ibrahim, M. Tache, and T.-J. King Liu**	**On Ultra-Low Power Hybrid NEMS-CMOS**	**IEEE International Conference on Nanotechnology**	**Toronto, ON, Canada**	**18-21 Aug. 2014**	**201 - 206**
	Journal	**A**	**8**	**8**		Y. Qian et al.	Pull-In Voltage and Fabrication Yield Analysis of All-Metal-Based Nanoelectromechanical Switches	**Journal of Microelectromechanical Systems**	Vol. 24, No. 6	Dec. 2015	1878 - 1886
4.00			**8**	**8**	**4.00**						
C178	**CAS-14**					**V. Beiu, M. Tache, and F. Kharbash**	**Reliability Enhanced SRAM Bit-Cells**	**IEEE International Semiconductor Conference**	**Sinaia, Romania**	**13-15 Oct. 2014**	**229 - 232**
	PhD	**D**	**1**	**0**		H.K.O. Berge	Improvements towards Optimal Design of Reliable Subthreshold Digital CMOS with applications in Logic and Memory	Faculty of Mathematics and Natural Sciences, University of Oslo (No. 1658)	Oslo, Norway	15 Jul. 2015	1 - 111
1.00			**1**	**0**	**0.00**						
Ch01	**Chp. 18**					**V. Beiu**	**Optimal VLSI Implementations of Neural Networks**	**In J.G. Taylor (Ed.): Neural Networks and Their Applications**	**John Wiley & Sons**	**1996**	**255 - 276**
	IWANN-97	**B**	**4**	**4**		S. Draghici and I.K. Sethi	On the possibilities of the limited precision weights neural networks in classification problems	International Work-Conference on Artificial and Natural Neural Networks (LNCS 1240)	Lanzarote, Spain	4-6 Jun. 1997	753 - 762
	Journal	**A**	**8**	**8**		G.P.J. Schmitz, and C. Aldrich	Combinatorial Evolution of Regression Nodes in Feedforward Neural Networks	**Neural Networks**	Vol. 12, No. 1	Jan. 1999	175 - 189
	Journal	**A**	**8**	**8**		D. Braendler et al.	Deterministic Bit-Stream Digital Neurons	**IEEE Transactions on Neural Networks**	Vol. 13, Nov. 6	Nov. 2002	1514 - 1525
20.00			**20**	**20**	**20.00**						
Ch02	**Chp. E1.4**					**V. Beiu**	**Digital Integrated Circuit Implementations (of Neural Networks)**	**In E. Fiesler, and R. Beale (Eds.): Handbook of Neural Computations**	**Institute of Physics, New York, NY, USA**	**1996**	**E1.4 (1 - 34)**
	PhD	**D**	**1**	**0**		F. Elie	Conception et Realisation d'un Systeme Utilisant des Reseaux de Neurones pour l'Identification et la Caracterisation, a Bord de Sattelites, de Signaux Transitoires de Type Sifflement	University of Orleans	Orleans, France	23 Dec. 1997	1 - 178
	Journal	**A**	**8**	**8**		I. Bayraktaroglu et al.	ANNSyS: An Analog Neural Network Synthesis System	**Neural Networks**	Vol. 12, No. 2	Mar. 1999	325 - 338
	Chp. 12B	**B**	**4**	**4**		A. Schmid and D. Mlynek	Neural Networks and Fuzzy-Based Integrated Circuit and System Solutions Applied to the Biomedical Field	In H.-N. Teodorescu et al. (Eds.): Fuzzy and Neuro-fuzzy Systems in Medicine	CRC Press	1999	361 - 390

	PhD	**D**	**1**	**0**		D. Braendler	Implementing Neural Hardware with On Chip Training on Field Programmable Gate Arrays	Swinburne University of Technology	Melbourne, Australia	Feb. 2002	1 - 312
	Journal	**A**	**8**	**8**		S. Draghici	On the Capabilities of Neural Networks Using Limited Precision Weights	**Neural Networks**	Vol. 15, No. 3	Apr. 2002	395 - 414
	IJCNN-03	**A**	**8**	**8**		S. Badel et al.	A VLSI Hamming Artificial Neural Network with k-Winner-Take-All and k-Loser-Take-All Capability	IEEE International Joint Conference on Neural Networks	Portland, OR, USA	Jul. 2003	977 - 982
	PhD	**D**	**1**	**0**		L. Brunelli	Abordagem para Reducao de Complexidade de RNA usando Reconfiguracao Dinamica	Universidade Federal de Campina Grande	Campina Grande, Paraiba, Brasil	Feb. 2005	1 - 184
	IJCNN-05	**A**	**8**	**8**		L. Brunelli et al.	A Novel Approach to Reduce Interconnect Complexity in ANN Hardware Implementation	IEEE International Joint Conference on Neural Networks	Montreal, Canada	31 Jul. - 4 Aug. 2005	2861- 2866
	PhD	**D**	**1**	**0**		F. Schurmann	Exploring Liquid Computing in a Hardware Adaptation: Construction and Operation of a Neural Network Experiment	Kirchhoff Institut fur Physik, Ruprecht-Karls-Universitat Heidelberg	Heidelberg, Germany	8 Jun. 2005	1 - 200
	Journal	**B**	**4**	**4**		R. Al-Alawi	Performance Evaluation of Fuzzy Single Layer Weightless Neural Network	**International Journal of Uncertainty, Fuzziness and Knowledge-Based Systems**	Vol. 15, No. 3	Jun. 2007	381 - 393
	ICANN-07	**B**	**4**	**4**		G. Lappas	Estimating the Size of Neural Networks from the Number of Available Training Data	International Conference on Artificial Neural Networks (LNCS 4668)	Porto, Portugal	9-13 Sept. 2007	68 - 77
	Journal	**C**	**2**	**0**		S. Badel et al.	CMOS Realization of Two-Dimensional Mixed Analog-Digital Hamming Distance Discriminator Circuits for Real-Time Imaging Applications	**Microelectronics Journal**	Vol. 39, No. 12	Dec. 2008	1817 - 1828
	acm	**D**	**1**	**0**		G. Lappas	Neural Networks and Multimedia Datasets: Estimating the Size of Neural Networks for Achieving High Classification Accuracy	WSEAS International Conference on Multimedia Systems & Signal Processing	Hangzhou, China	20-22 May 2009	237 - 242
	Journal	**D**	**1**	**0**		G. Lappas	Designing Neural Networks for Tackling Hard Classification Problems	**WSEAS Transactions on Systems**	Vol. 8, No. 6	Jun. 2009	743 - 752
	Journal	**B**	**4**	**4**		L. Leiva and N. Acosta	Hardware Radial Basis Function Neural Network Automatic Generation	**Journal of Computer Science & Technology**	Vol. 11, No. 1	Apr. 2011	15 - 20
	Journal	**B**	**4**	**4**		N. Izeboudjen et al.	A New Classification Approach for Neural Networks Hardware: From Standards Chips to Embedded Systems on Chip	**Artificial Intelligence Review**	Vol. 41, No. 4	Apr. 2014	491 - 534
60.00			**60**	**52**	**52.00**						

Ch03	**Chp. 12**					**V. Beiu**	**Constant Fan-in Discrete Neural Networks Are VLSI-Optimal**	**In S.W. Ellacott, J.C. Mason, and I.J. Anderson (Eds.): Mathematics of Neural Networks Models, Algorithms and Applications**	**Kluwer Academic**	**1997**	**89 - 94**
	IJCNN-98	**A**	**8**	**8**		S. Draghici	Using Information Entropy Bounds to Design VLSI Friendly Neural Networks	IEEE International Joint Conference on Neural Networks	Ankorage, AK, USA	4-9 May 1998	547 - 552
	Journal	**A**	**8**	**8**		S. Draghici	On the Capabilities of Neural Networks Using Limited Precision Weights	**Neural Networks**	Vol. 15, No. 3	Apr. 2002	395 - 414
	PhD	**D**	**1**	**0**		L. Brunelli	Abordagem para Reducao de Complexidade de RNA usando Reconfiguracao Dinamica	Universidade Federal de Campina Grande	Campina Grande, Paraiba, Brasil	Feb. 2005	1 - 184
17.00			**17**	**16**	**16.00**						

Ch04	**Chp.**					**V. Beiu**	**Entropy, Constructive Neural Learning, and VLSI Efficiency**	**In R. Andonie, and D. Grosu (Eds.): Neural Priorities in Data Transmission and EDA. Tempus SJEP 8180-94**	**Transilvania" Univ. of Braşov Press, Braşov, Romania**	**1998**	**38 - 74**
	scitech	**D**	**1**	**0**		H.E. Makaruk	Computations of Entropy Bounds: Multidimensional Geometric Methods	Los Alamos National Laboratory LA-UR--97-4413	DOE, USA	Feb. 1998	1 - 10
	Book	**B**	**4**	**4**		M.N. Cristea et al.	Neural and Fuzzy Logic Control of Drives and Power Systems	Elsevier	Oxford, UK	Jul. 2002	1 - 399
5.00			**5**	**4**	**4.00**						
Ch05	**Chp. 12**					**V. Beiu, and W. Ibrahim**	**On Computing Nano-Architectures Using Unreliable Nano-Devices**	**In S.E. Lyshevski (Ed.): Nano- and Molecular-Electronics Handbook**	**CRC Press / Taylor & Francis**	**May 2007**	**1 - 49**
	Chp. 5	**B**	**4**	**4**		S. Das et al.	System-Level Design and Simulation of Nanomemories and Nanoprocessors	In "Nano and Molecular Electronics Handbook," CRC Press	USA and UK	May 2007	1 - 39
	ieee	**D**	**1**	**0**		W. Ibrahim et al.	A Bayesian Based EDA Tool for Accurate VLSI Reliability Evaluations	IEEE International Conference on Innovations in Information Technology	Al Ain, UAE	16-18 Dec. 2008	101 - 105
	ieee	**D**	**1**	**0**		A. Beg and W. Ibrahim	Relating Reliability to Circuit Topology	IEEE North-East Workshop on Circuits and Systems	Toulouse, France	28 Jun. - 1 Jul. 2009	5290421 (1-4)
	ebscohost	**D**	**1**	**0**		J. Wade et al.	Self-repair in a Bidirectionally Coupled Astrocyte-Neuron (AN) System Based on Retrograde Signaling	**Frontiets in Computational Neuroscience (ISI IF = 2.653)**	Vol. 6	Sept. 2012	76 (1-12)
	Journal	**A**	**8**	**8**		W. Ibrahim et al.	Accurate and Efficient Estimation of Logic Circuits Reliability Bounds	**IEEE Transactions on Computers**	Vol. 64, No. 5	May 2015	1217 - 1229
	Journal	**A**	**8**	**8**		W. Ibrahim	Identifying the Worst Reliability Input Vectors and the Associated Critical Logic Gates	**IEEE Transactions on Computers**	Vol. 65, No. 6	Jul. 2016	1748 - 1760
	SCSC-16	**B**	**4**	**4**		W. Ibrahim and H. Amer	Critical nodes count algorithm for accurate input vectors reliability ranking	International Summer Computer Simulation Conference	Montreal, Quebec, Canada	24-27 Jul. 2016	art. 19 (http://dl.acm.org/citation.cfm?id=3015593)
27.00			**27**	**24**	**24.00**						
Ch07	**Chp. 6**					**A. Beg, M.H. Sulieman, V. Beiu, and W. Ibrahim**	**Low-Power Reliable Nano Adders**	**In J.E. Morris and K. Iniewski (Eds.): Nanoelectronic Device Applications Handbook**	**CRC Press / Taylor & Francis**	**Jun. 2013**	**67 - 75**
	CSCWD-13	**B**	**4**	**4**		A. Beg et al.	A Collaborative Platform for Facilitating Standard Cell Characterization	IEEE International Conference on Computer Supported Cooperative Work in Design	Whistler, BC, Canada	Jun. 2013	202 - 206
2.00			**4**	**4**	**2.00**						
J005	**Journal**					**V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins**	**Close Approximations of Sigmoid Functions by Sum of Steps for VLSI Implementation of Neural Networks**	**Scientific Annals of Computer Science "Al. I. Cuza" University of Iaşi**	**vol. 40, no. 3**	**1994**	**5 - 34**
	PARLE-94	**C**	**2**	**0**		O. Brudaru and G.M. Megson	Systolic Designs for Evaluating Linear Combinations of Chebyshev Polynomials	International Conference on Parallel Architectures and Languages Europe (LNCS 817)	Athens, Greece	4-8, Jul. 1994	502 - 513

	ieee	D	1	0		M.A. Zohdy and A.A. Zaher	Hybrid Dynamic Neural Learning (HDNL) in Control Applications	IEEE Midwest Symposium on Circuits and Systesm	Dayton, OH, USA	14-17 Aug. 2001	627 - 635
	Chp. 10	B	4	4		A. Canas et al.	FPGA Implementation of a Fully and Partially Connected MLP: Applications to Automatic Speech Recognition	In A.R. Omondi and J.C. Rajapakse (Eds.): "FPGA Implementations of Neural Networks"	Springer	Oct. 2006	271 - 296
	ieee	D	1	0		S. Jeyanthi and M. Subadra	Implementation of single neuron using various activation functions with FPGA	International Conference on Advanced Communication Control and Computing Technologies (ICACCCT)	Tamilnadu, India	8-10 May 2014	1126 - 1131
	Journal	D	1	0		M. Sulaiman et al.	New Methodology for Chattering Suppression of Sliding Mode Control for Three-phase Induction Motor Drives	**WSEAS Transactions on Systems and Control**	Vol. 9	2014	1 - 9
	ProQuest	D	1	0		A.T. Oladipo and O.A. Fadipe-Joseph	Iterated Integral Transforms of Activated Sigmoid Function as Related to Caratheodory Family	**Far East Journal of Applied Mathematics**	Vol. 94, No. 1	Jan. 2016	1 - 15
5.00			**10**	**4**	**2.00**						

J006	**Journal**					**V. Beiu**	**Entropy Bounds for Classification Algorithms**	**Neural Network World**	**vol. 6, no. 4**	**Jul. 1996**	**497 - 505**
	IWANN-97	B	4	4		S. Draghici and I.K. Sethi	On the possibilities of the limited precision weights neural networks in classification problems	International Work-Conference on Artificial and Natural Neural Networks (LNCS 1240)	Lanzarote, Spain	4-6 Jun. 1997	753 - 762
	Chapter	D	1	0		P. Moerland and E. Fiesler	Neural Network Adaptations to Hardware Implementations	Handbook of Neural Computations	IoP & Oxford Univ.Press	Jan. 1997	E1.2 1 - 13
	scitech	D	1	0		H.E. Makaruk	Computations of Entropy Bounds: Multidimensional Geometric Methods	Los Alamos National Laboratory LA-UR--97-4413	DOE, USA	Feb. 1998	1 - 10
	IJCNN-99	A	8	8		S. Draghici	Some New Results on the Capabilities of Integer Weights Neural Networks in Classification Problems	IEEE International Joint Conference on Neural Networks	Washington, DC, USA	10-16 Jul. 1999	519 - 524
	PhD	D	1	0		D. Braendler	Implementing Neural Hardware with On Chip Training on Field Programmable Gate Arrays	Swinburne University of Technology	Melbourne, Australia	Feb. 2002	1 - 312
	Journal	A	8	8		S. Draghici	On the Capabilities of Neural Networks Using Limited Precision Weights	**Neural Networks**	Vol. 15, No. 3	Apr. 2002	395 - 414
23.00			**23**	**20**	**20.00**						

J007	**Journal**					**V. Beiu, and J.G. Taylor**	**On the Circuit Complexity of Sigmoid Feedforward Neural Networks**	**Neural Networks**	**vol. 9, no. 7**	**Oct. 1996**	**1155 - 1171**
	CiteSeerX	D	1	0		P.J.L. Adeodato and J.G. Taylor	Storage Capacity of RAM-based Neural Networks: Pyramids	Workshop on Neural Networks		1996	103 - 110
	Chapter	D	1	0		R. Andonie	The "Psychological" Limits of Neural Computation	In M. Kárný, K. Warwick, and V. Kůrková (Eds.): "Dealing with Complexity: A Neural Networks Approach"	Springer	Dec. 1997	252 - 263
	PhD	D	1	0		D. Husmeier	Modelling Conditional Probability Densities with Neural	King's College London	London,UK	Dec. 1997	1 - 307
	scitech	D	1	0		H.E. Makaruk	Computations of Entropy Bounds: Multidimensional Geometric	Los Alamos National Laboratory LA-UR--97-4413	DOE, USA	Feb. 1998	1 - 10
	Journal	A	8	8		S. Draghici	On the Capabilities of Neural Networks Using Limited Precision	**Neural Networks**	Vol. 15, No. 3	Apr. 2002	395 - 414
	IWANN-03	B	4	4		M. Padure et al.	CMOS Implementation of Generalized Threshold Functions	International Work-Conference on Artificial and Natural Neural	Maó, Menorca,	3-6 Jun. 2003	65 - 72
	Book	B	4	4		K.-L. Du and	Neural Networks in a Softcomputing Framework	Springer	London, UK	May 2006	1 - 566
	ICANN-07	B	4	4		R. Eickhoff et al.	Impact of Shrinking Technologies on the Activation Function of	International Conference on Artificial Neural Networks (LNCS	Porto, Portugal	9-13 Sept.	501 - 510
	Journal	A	8	8		J.L. Subirats et	A New Decomposition Algorithm for Threshold Synthesis and	**IEEE Transactions on Circuits and Systems I**	Vol. 55, No. 10	Nov. 2008	3188 - 3196
	PhD	D	1	0		M.K. Goparaju	Coping with Discrepancies of the Manufactured Weights in Threshold Logic Gates (UMI 3390854)	Southern Illinois University Carbondale	Carbondale, IL, USA	Dec. 2009	1 - 75
	PhD	D	1	0		J.L. Subirats	Diseño de algoritmos constructivos de redes neuronales para la síntesis de arquitecturas con gran capacidad de generalización	Universidad de Málaga	Málaga, Spain	May 2013	1 - 189
	Chp. 23	B	4	4		K.-L. Du and M.N.S. Swamy	Neural Circuits and Parallel Implementation	In K.-L. Du and M.N.S. Swamy "Neural Networks and Statistical Learning"	Springer	Dec. 2013	705 - 725

38.00			**38**	**32**	**32.00**						
J008	**Journal**					**V. Beiu**	**Reduced Complexity Constructive Learning Algorithm**	**Neural Network World**	**vol. 8, no. 1**	**Jan. 1998**	**1 - 38**
	PhD	**D**	**1**	**0**		J. Sima	Neuronové Síte Jako Modely Analogových Výpoctu	Academy of the Czech Republic	Prague, Czech Republic	Apr. 2006	1 - 46
1.00			**1**	**0**	**0.00**						
J009	**Journal**					**V. Beiu**	**On the Circuit and VLSI Complexity of Threshold Gate COMPARISON**	**Neurocomputing**	**vol. 19, no. 1**	**Apr. 1998**	**77 - 98**
	IlliGAL	**D**	**1**	**0**		D.E. Goldberg	Genetic Algorithms: A Bibliography	Univ. of Illinois at Urbana-Champaign, Illinois Genetic Algorithms Laboratory (IlliGAL), Tech. Rep. 2000037	Urbana-Champaign, IL, USA	Jan. 2000	1 - 380
	Journal	**A**	**8**	**8**		S. Draghici	On the Capabilities of Neural Networks Using Limited Precision Weights	**Neural Networks**	Vol. 15, No. 3	Apr. 2002	395 - 414
	ieee	**D**	**1**	**0**		M. Stankovic et al.	Mapping Decision Diagrams for Multiple-Valued Logic Functions into Threshold Logic Networks	IEEE International Symposium on Multiple-Valued Logic	Tuusula, Finland	23-25 May 2011	111 - 116
	ieee	**D**	**1**	**0**		B. Hanindhito et al.	FPGA Implementation of Modified Serial Montgomery Modular Multiplication for 2048-bit RSA Cryptosystems	IEEE International Seminar on Intelligent Technology and Its Applications	At Surabaya, Indonesia	20-21 May 2015	113 - 117
11.00			**11**	**8**	**8.00**						
J010	**Journal**					**V. Beiu, and H.E. Makaruk**	**Deeper Sparsely Nets Can Be Optimal**	**Neural Processing Letters**	**vol. 8, no. 3**	**Dec. 1998**	**201 - 210**
	Chapter	**D**	**1**	**0**		R. Andonie	The "Psychological" Limits of Neural Computation	In M. Kárný, K. Warwick, and V. Kürková (Eds.): "Dealing with Complexity: A Neural Networks Approach"	Springer	Dec. 1997	252 - 263
	Journal	**A**	**8**	**8**		S. Draghici	On the Capabilities of Neural Networks Using Limited Precision Weights	**Neural Networks**	Vol. 15, No. 3	Apr. 2002	395 - 414
	IWANN-03	**B**	**4**	**4**		S. Aunet and Y. Berg	UV-programmable Floating-Gate CMOS Linear Threshold Element "P1N3"	International Work-Conference on Artificial and Natural Neural Networks (LNCS 2687)	Maó, Menorca, Spain	3-6 Jun. 2003	57 - 64
	Journal	**A**	**8**	**8**		S. Aunet et al.	Real-Time Reconfigurable Linear Threshold Elements Implemented in Floating-Gate CMOS	**IEEE Transactions on Neural Networks**	Vol. 14, No. 5	Sept. 2003	1244 - 1256
	IJCNN-04	**A**	**8**	**8**		S. Aunet et al.	Reconfigurable Subthreshold CMOS Perceptron	IEEE International JointConference on Neural Networks	Budapest, Hungary	25-29 Jul. 2004	1983 - 1988
	Journal	**A**	**8**	**8**		S. Aunet et al.	Real-Time Reconfigurable Subthreshold CMOS Perceptron	**IEEE Transactions on Neural Networks**	Vol. 19, No. 4	Apr. 2008	645 - 657
	ieee	**D**	**1**	**0**		A. Amarnath et al.	Latency and Power Consumption in Unstructured Nanoscale Boolean Networks	IEEE International Conference on Nanotechnology	Portland, OR, USA	15-18 Aug. 2011	854 - 859
	Journal	**B**	**4**	**4**		A.K. Palaniswamy and S. Tragoudas	An Efficient Heuristic to Identify Threshold Logic Functions	**ACM Journal on Emerging Technologies in Computing**	Vol. 8, No. 3	Aug. 2012	19 (1 - 17)
	Chp. 13	**B**	**4**	**4**		C. Teuscher	Computation and Communication in Unorganized Systems	In H. Zenil (ed.): A Computable Universe - Understanding and Exploring Nature as Computation	World Scientific	Dec. 2012	231 - 242
46.00			**46**	**44**	**44.00**						
J011	**Journal**					**V. Beiu, S. Draghici, and T. De Pauw**	**A Constructive Approach to Calculating Lower Entropy Bounds**	**Neural Processing Letters**	**vol. 9, no. 1**	**Feb. 1999**	**1 - 12**
	IJCNN-99	**A**	**8**	**8**		S. Draghici	Some New Results on the Capabilities of Integer Weights Neural Networks in Classification Problems	IEEE International Joint Conference on Neural Networks	Washington, DC, USA	10-16 Jul. 1999	519 - 524

	Journal	**A**	**8**	**8**		S. Draghici	On the Capabilities of Neural Networks Using Limited Precision Weights	**Neural Networks**	Vol. 15, No. 3	Apr. 2002	395 - 414
16.00			**16**	**16**	**16.00**						
J014						**V. Beiu, J.M. Quintana, and M.J. Avedillo**	**VLSI Implementations of Threshold Gates — A Comprehensive Survey**	**IEEE Transactions on Neural Networks**	**vol. 14, no. 5**	**May 2003**	**1217 - 1243**
	semantic	**D**	**1**	**0**		D. Bhaduri and S. Shukla	Comparing Reliability-Redundancy Trade-offs for Two von Neumann Multiplexing Architectures	FERMAT Tech. Rep. 2005-01, VirginiaTech	Semantic Scholar, Allen Inst. AI	2005	1 - 22
	IWANN-03	**B**	**4**	**4**		S. Aunet and Y. Berg	UV-programmable Floating-Gate CMOS Linear Threshold Element "P1N3"	International Work-Conference on Artificial and Natural Neural Networks (LNCS 2687)	Maó, Menorca, Spain	3-6 Jun. 2003	57 - 64
	ieee	**D**	**1**	**0**		J.M. Quintana et al.	Design of Residue Generators Using Threshold Logic	IEEE International Midwest Symposium on Circuits and Systems	Cairo, Egypt	27-30 Dec. 2003	1427 - 1430
	IJCNN-04	**A**	**8**	**8**		S. Aunet et al.	Reconfigurable Subthreshold CMOS Perceptron	IEEE International Joint Conference on Neural Networks	Budapest, Hungary	25-29 Jul. 2004	1983 - 1988
	Journal	**B**	**4**	**4**		M.J. Avedillo et al.	Pass-transistor Based Implementations of Threshold Logic Gates for WOS Filtering	**Microelectronics Journal**	Vol. 35, No. 11	Nov. 2004	869 - 873
	Book	**B**	**4**	**4**		K. Goser et al.	Nanoelectronics and Nanosystems: From Transistors to Molecular and Quantum Devices	Springer	Berlin Heidelberg	2004	1 - 281
	ieee	**D**	**1**	**0**		P. Gupta et al.	An Automatic Test Pattern Generation Framework for Combinational Threshold Logic Networks	IEEE International Conference on Computer Design	San Jose, USA	11-13 Oct. 2004	540 - 543
	cordis.eu	**D**	**1**	**0**		W. Prost	QUDOS Quantum Tunnelling Devices Technology on Silicon	Quantum Tunnelling Device Technology on Silicon	Brussels, Belgium	27 Oct. 2004	1 - 80
	PhD	**D**	**1**	**0**		T.R. Surmacz	Metody generowania minimalnego zbioru testów dla pewnych klas sieci sortujacych	Wroclaw University	Wroclaw, Poland	2004	1 - 135
	ieee	**D**	**1**	**0**		R. Zhang et al.	Synthesis and Optimization of Threshold Logic Networks with Application to Nanotechnologies	IEEE International Conference on Design, Automation and Test in Europe	Paris, France	16-20 Feb. 2004	904 - 909
	WO2005057789	**D**	**1**	**0**		S. Aunet	Circuit Element	Leiv Eiriksson Nyskaping AS		23 Jun. 2005	http://www.google.com/patents/WO2005057789A1
	ieee	**D**	**1**	**0**		V. Brea et al.	Robustness Improvement in Binary Cellular Non-linear Network Architectures	IEEE European Conference on Circuit, Theory and Design	Cork, Ireland	Aug. 29 - Sep. 2	149 - 152
	ieee	**D**	**1**	**0**		L. Rozenblyum and A. Kondratyev	Tribute to Victor Varshavsky	IEEE International Symposium on Asynchronous Circuits and Systems	New York, NY, USA	13-16 Mar. 2005	1 - 36
	PhD	**D**	**1**	**0**		F. Schurmann	Exploring Liquid Computing in a Hardware Adaptation: Construction and Operation of a Neural Network Experiment	Kirchhoff Institut fur Physik, Ruprecht-Karls-Universitat Heidelberg	Heidelberg, Germany	8 Jun. 2005	1 - 200
	Journal	**B**	**4**	**4**		R. Zhang et al.	Threshold Network Synthesis and Optimization and Its Application to Nanotechnologies	**IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**	Vol. 24, No. 1	Jan. 2005	107 - 118
	ieee	**D**	**1**	**0**		D. Bol et al.	Monostable-Bistable Transition Logic Elements: Threshold Logic vs. Boolean Logic Comparison	IEEE International Conference on Electronics, Circuits and Systems	Nice, France	10-13 Dec. 2006	1049 - 1052
	ieee	**D**	**1**	**0**		M. Ferringer et al.	VLSI Implementation of a Fault-tolerant Distributed Clock Generation	IEEE Symposium on Defect and Fault Tolerance in VLSI Systems	Washington, DC, USA	4-6 Oct. 2006	563 - 571
	PhD	**D**	**1**	**0**		J. Fieres	A Method for Image Classification Using Low-precision Analog Elements	Kirchhoff Institut fur Physik, Ruprecht-Karls-Universitat Heidelberg	Heidelberg, Germany	29 Nov. 2006	1 - 147

ieee	D	1	0	W. Kuang and E. Banatoski	Testing for Threshold Logic Circuits Based on Resonant Tunneling Diodes	IEEE International Conference on Nanotechnology	Cincinnati, OH, USA	16-20 Jul. 2006	387 - 390
WCCI-06	A	8	8	R. Neville	A Hardware Implementation of Multi-level Threshold Logic for Artificial Neural Net	IEEE World Congress on Computational Intelligence	Vancouver, Canada	16-21 Jul. 2006	2845 - 2851
Journal	A	8	8	P. Oikonomou and P. Cluzel	Effects of Topology on Network Evolution	**Nature Physics**	Vol. 2	Aug. 2006	532 - 536
PhD	D	1	0	P. Patronik	Metody syntezy ukladów realizujacych funkcje symetryczne I progowe testowalnych dla uszkodzen typu opóznienia	Wroclaw University	Wroclaw, Poland	2006	1 - 127
PhD	D	1	0	G.R. Roelke	Fault and Defect Tolerant Computer Architectures: Reliable Computing With Unreliable Devices	Air Force Institute of Technology	Wright-Patterson, OH, USA	Sept. 2006	1 - 421
ICANN-06	B	4	4	J.L. Subirats et al.	Optimal Synthesis of Boolean Functions by Threshold Functions	International Conference on Artificial Neural Networks (LNCS 4131)	Athens, Greece	10-14 Sept. 2006	983 - 992
PhD	D	1	0	R. Zhang	Computer-Aided Design Algorithm and Tools for Nanotechnologies	EE Department, Princeton University	Princeton, NJ, USA	Nov. 2006	1 - 157
Journal	B	4	4	K. Aoyama	Design Methods for Symmetric Function Generators Based on Threshold Elements	**IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**	Vol. 26, No. 11	Nov. 2007	1934 - 1946
US 7,288,968	D	1	0	S. Aunet	Circuit Element	Leiv Eiriksson Nyskaping AS	Washington, DC, USA	30 Oct. 2007	1 - 11
PhD	D	1	0	Y. Benedic	Approche Analytique pour l'Optimisation de Reseaux de Neurones Artificiels (in French)	Universite de Haute-Alsace	Mulhouse, France	11 Dec. 2007	1 - 220
ieee	D	1	0	K.S. Berezowski and S.B.K. Vrudhula	Multiple-Valued Logic Circuits Design using Negative Differential Resistance Devices	IEEE International Symposium on Multiple-Valued Logic	Oslo, Norway	14-15 May 2007	4215947 (1 - 7)
Journal	B	4	4	K.S. Berezowski and S.B.K. Vrudhula	Multiple-Valued Logic Circuits Design using Negative Differential Resistance Devices	**Journal of Multiple-Valued Logic and Soft Computing**	Vol. 13, No. 4-6	2007	447 - 466
ieee	D	1	0	V.M. Brea et al.	Relating Cellular Non-linear Networks to Threshold Logic and Single Instruction Multiple Data Computing Models	IEEE European Conference on Circuit Theory and Design	Seville, Spain	27-30 Aug. 2007	92 - 95
ieee	D	1	0	A. Djupdal and P.C. Haddow	Defect Tolerant Ganged CMOS Minority Gate	IEEE Norchip International Conference	Aalborg, Denmark	19-20 Nov. 2007	4481060 (1 - 4)
ieee	D	1	0	M.K. Goparaju and S. Tragoudas	A Fault Tolerant Design Methodology for Threshold Logic Gates and Its Optimizations	IEEE International Symposium on Quality Electronic Design	San Jose, CA, USA	26-28 Mar. 2007	420 - 425
acm	D	1	0	T. Gowda et al.	Combinational Equivalence Checking for Threshold Logic Circuits	ACM International Great Lakes Symposium on VLSI	Stresa, Italy	11-13 Mar. 2007	102 - 107
Journal	B	4	4	S. Kaya et al.	Reconfigurable Threshold Logic Gates with Nano-scale DG-MOSFETs	**Solid-State Electronics**	Vol. 51, No. 10	Oct. 2007	1301 - 1307
Journal	B	4	4	S.J. Piestrak	Efficient Hamming Weight Comparators of Binary Vectors	**Electronics Letters**	Vol. 43, No. 11	24 May 2007	611 - 612
Journal	B	4	4	G.R. Roelke at al.	A Cache Architecture for Extremely Unreliable Nanotechnologies	**IEEE Transactions on Reliability**	Vol. 56, No. 2	Jun. 2007	182 - 197
Journal	A	8	8	J. Sitte et al.	Characterization of Analog Local Cluster Neural Network Hardware for Control	**IEEE Transactions on Neural Networks**	Vol. 18, No. 4	Jul. 2007	1242 - 1253
Journal	A	8	8	J. Sköldberg and G. Wendin	Reconfigurable Logic in Nanoelectronic Switching Networks	**Nanotechnology**	Vol. 18, No. 48	5 Dec. 2007	485201 (1 - 10)
springer	D	1	0	G. Tufte and P.C. Haddow	Extending Artificial Development: Exploiting Environmental Information for the Achievement of Phenotypic Plasticity	International Conference on Evolvable Systems: From Biology to Hardware (LNCS 4684)	Wuhan, China	21-23 Sept. 2007	297 - 308

ieee	D	1	0	G. Tufte and P.C. Haddow	Achieving Environmental Tolerance through the Initiation and Exploitation of External Information	IEEE Congress on Evolutionary Computation	Singapore	25-28 Sept. 2007	2485 - 2492
Journal	**A**	**8**	**8**	S. Aunet et al.	Real-Time Reconfigurable Subthreshold CMOS Perceptron	**IEEE Transactions on Neural Networks**	Vol. 19, No. 4	Apr. 2008	645 - 657
PhD	**D**	**1**	**0**	A. Djupdal	Evolving Static Hardware Redundancy for Defect Tolerant FPGAs	Norwegian University of Science and Technology	Trondheim, Norway	25 Apr. 2008	1 - 124
Journal	**A**	**8**	**8**	J. Freixas and X. Molinero	The Greatest Allowed Relative Error in Weights and Threshold of Strict Separating Systems	**IEEE Transactions on Neural Networks**	Vol. 19, No. 5	May 2008	770 - 781
ieee	D	1	0	G. Fuchs et al.	Mapping a Fault-Tolerant Distributed Algorithm to Systems on Chip	IEEE EuroMicro Conference on Digital System Design DSD-08	Parma, Italy	3-5 Sept. 2008	242 - 249
ieee	D	1	0	S.R.S. Garimella et al.	Low Depth Carry Look Ahead Circuits using Rail-to-Rail Capacitive Threshold Logic	IEEE International Midwest Symposium on Circuits and Systems	Knoxville, TN, USA	10-13 Aug. 2008	574 - 577
ieee	D	1	0	M.K. Goparaju and S. Tragoudas	A Novel ATPG Framework to Detect Weight Related Defects in Threshold Logic Gates	IEEE International VLSI Test Symposium	San Diego, CA, USA	27 Apr. - 1 May 2008	323 - 328
ieee	D	1	0	M.K. Goparaju et al.	A Fault Tolerance Aware Synthesis Methodology for Threshold Logic Gate Networks	IEEE International Symposium on Defect and Fault Tolerance of VLSI Systems	Cambridge, MA, USA	1-3 Oct. 2008	176 - 183
ieee	D	1	0	T. Gowda et al.	Decomposition Based Approach for Synthesis of Multi-Level Threshold Logic Circuits	IEEE International Asia and South Pacific Design Automation Conference	Seoul, South Korea	21-24 Mar. 2008	125 - 130
PhD	**D**	**1**	**0**	H. Gundersen	Aspects of Balanced Ternary Arithmetics Implemented Using CMOS Recharged Semi-Floating Gate Devices	University of Oslo	Oslo, Norway	17 Jun. 2008	1 - 114
Journal	**B**	**4**	**4**	P. Gupta et al.	Automatic Test Generation for Combinational Threshold Logic Networks	**IEEE Transactions on VLSI Systems**	Vol. 16, No. 8	Aug. 2008	1035 - 1045
PhD	**D**	**1**	**0**	M. He	Contribution à l'étude de l'impact des nanotechnologies sur les architectures : Apprentissage d'inspiration neuronale de fonctions logiques pour circuits programmables	Université de Paris Sud XI	Orsay, France	17 Dec. 2008	1 - 159
Book	**B**	**4**	**4**	M.G. Karpovsky et al.	Spectral Logic and Its Applications for the Design of Digital Devices	J. Wiley & Sons	Hoboken, NJ, USA	2008	1 - 592
Journal	**A**	**8**	**8**	M. Laiho et al.	Template Design for Cellular Nonlinear Networks With 1-Bit Weights	**IEEE Transactions on Circuits and Systems I**	Vol. 55, No. 3	Apr. 2008	904 - 913
Journal	**B**	**4**	**4**	S.E. Lyshevski et al.	Computing Paradigms for Logic Nanocells	**Journal of Computational and Theoretical Nanoscience**	Vol. 5, No. 12	Dec. 2008	2377 - 2395
US 7,401,058	**D**	**1**	**0**	H.E. Michel and D.P. Rancour	Artificial Neuron with Phase-encoded Logic	**US Patent, University of Massachusetts**	Washington, DC, USA	15 Jul. 2008	1 - 15
PhD	**D**	**1**	**0**	P. Oikonomou	Application of Stochastic Processes in Random Growth and Evolutionary Dynamics (UMI 3338500)	University of Chicago	Chicago, IL, USA	Dec. 2008	1 - 139
asme	D	1	0	G. Shafat et al.	Using Threshold Functions in Teaching Electronics	Biennial ASME Conference on Engineering Systems, Design and Analysis	Haifa, Israel	7-9 Jul. 2008	1 - 5
Journal	**A**	**8**	**8**	J.L. Subirats et al.	A New Decomposition Algorithm for Threshold Synthesis and Generalization of Boolean Functions	**IEEE Transactions on Circuits and Systems I**	Vol. 55, No. 10	Nov. 2008	3188 - 3196
Chp. 17	**B**	**4**	**4**	M.B. Tahoori et al.	Testing Aspects of Nanotechnology Trends	In L.-T. Wang, C.E. Stroud, and N.A. Touba (Eds.): "System-on-Chip Test Architectures: Nanometer Design for Testability"	Elsevier / Morgan Kaufmann	2008	791 - 831
acm	D	1	0	G. Tufte	Phenotypic, Developmental and Computational Resources: Scaling in Artificial Development	ACM Genetic and Evolutionary Computation Conference	Atlanta, GA, USA	12-16 Jul. 2008	859 - 866
springer	D	1	0	G. Tufte	Discovery and Investigation of Inherent Scalability in Developmental Genomes	International Conference on Evolvable Systems: From Biology to Hardware (LNCS 5216)	Springer	2008	189 - 200

alifexi	D	1	0	G. Tufte	Evolution, Development and Environment Toward Adaptation through Phenotypic Plasticity and Exploitation of External Information	Artificial life XI	Winchester, UK	5-8 Aug. 2008	624 - 631
Book	B	4	4	L.-T. Wang, C.E. Stroud, and N.A. Touba	Systems on Silicon : System-on-Chip Test Architectures : Nanometer Design for Testability	Elsevier / Morgan Kaufmann	Burlington, MA, USA	2008	1 - 856
Chp. 24	B	4	4	R. Lauwereins and J. Madsen	Design, Automation, and Test in Europe: The Most Influential Papers of 10 Years DATE	Springer	Netherlands	January	1 - 516
PhD	D	1	0	G. Fuchs	Fault-Tolerant Distributed Algorithms for On-Chip Tick Generation: Concepts, Implementations and Evaluations	Technical University of Vienna	Vienna, Austria	Aug. 2009	1 - 163
PhD	D	1	0	M.K. Goparaju	Coping with Discrepancies of the Manufactured Weights in Threshold Logic Gates (UMI 3390854)	Southern Illinois University Carbondale	Carbondale, IL, USA	Dec. 2009	1 - 75
US/20090235216	D	1	0	T. Gowda and S. Vrudhula	Combinational Equivalence Checking for Threshold Logic Circuits	US Patent Application	Washington, DC, USA	17 Sept. 2009	1 - 23
ieee	D	1	0	S. Kaya et al.	Highly Reconfigurable and Error Tolerant Threshold Logic Gates Based on Nanoscale DG-MOSFETs	IEEE International Semiconductor Device Research Symposium	College Park, MD, USA	9-11 Dec. 2009	5378246 (1 - 2)
acm	D	1	0	S. Maltabas et al.	Varicap Threshold Logic	ACM Great Lakes Symposium on VLSI	Boston, MA, USA	10-12 May 2009	239 - 244
acm	D	1	0	A.K. Palaniswamy et al.	A Fault Tolerant Threshold Logic Gate Design	WSEAS International Conference on Circuits	Rodos, Greece	22-24 Jul. 2009	162 - 167
PhD	D	1	0	A. Patel	Noise Benefits in Nonlinear Signal Processing (UMI 3389532)	University of Southern California	Los Angeles, CA	Dec. 2009	1 - 245
Journal	A	8	8	A. Patel and B. Kosko	Error-Probability Noise Benefits in Threshold Neural Signal Detection	**Neural Networks**	Vol. 22, No. 5-6	Jul. 2009	697 - 706
Journal	D	1	0	C.P. Raj and S.L. Pinjare	Design and Analog VLSI Implementation of Neural Network Architecture for Signal Processing	**European Journal of Scientific Research**	Vol. 27, No. 2	Feb. 2009	199 - 216
Journal	A	8	8	R.M. Roth et al.	Defect-Tolerant Demultiplexer Circuits Based on Threshold Logic and Coding	**Nanotechnology**	Vol. 20, No. 13	1 Apr. 2009	135201 (1 - 14)
ieee	D	1	0	T. Shinogi et al.	Probabilistic Metric of Gate Logical Fault Occurrence Due to Manufacturing Inaccuracy of Threshold Logic Gates for Efficient Testing	IEEE International Conference on Design & Technology of Integrated Systems in Nanoscale Era	Cairo, Egypt	6-9 Apr. 2009	230 - 235
Journal	A	8	8	M. Stanisavljevic et al.	Optimization of the Averaging Reliability Technique Using Low Redundancy Factors for Nanoscale Technologies	**IEEE Transactions on Nanotechnology**	Vol. 8, No. 3	May 2009	379 - 390
ieee	D	1	0	G. Tufte	The Discrete Dynamics of Developmental Systems	IEEE Congress on Evolutionary Computation	Tronheim, Norway	18 - 21 May 2009	2209 - 2216
ieee	D	1	0	S. Aunet and A. Hasanbegovic	Memory Elements Based on Minority-3 Gates and Inverters Implemented in 90 nm CMOS	IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems	Vienna, Austria	14-16 Apr. 2010	267 - 272
ieee	D	1	0	O.K. Ekekon et al.	Power Minimization Methodology for VCTL Topologies	IEEE International SOC Conference	Las Vegas, NV, USA	27-29 Sept. 2010	330 - 333
ICAART-10	C	2	0	J. Freixas and X. Molinero	Maximum Tolerance and Maximum Greatest Tolerance -- Weights and Threshold of Strict Separating Systems	International Conference on Agents and Artificial Intelligence	Valencia, Spain	22-24 Jan 2010	511 - 514
PhD	D	1	0	S. Leshner	Modeling and Implementation of Threshold Logic Circuits and Architectures (UMI 3428443)	**Arizona State University**	Tempe, AZ, USA	Nov. 2010	1 - 182
ieee	D	1	0	S. Leshner et al.	A Low Power, High Performance Threshold Logic-based Standard Cell Multiplier in 65nm CMOS	IEEE Computer Society Annual Symposium on VLSI	Lixouri Kefalonia, Greece	5-7 Jul. 2010	210 - 215

ieee	D	1	0	S. Leshner et al.	Design of a Robust, High Performance Standard Cell Threshold Logic Family for DSM Technology	IEEE International Conference on Microelectronics	Cairo, Egypt	19-22 Dec. 2010	52 - 55
acm	D	1	0	A.K. Palaniswamy et al.	Scalable Identification of Threshold Logic Functions	ACM Great Lakes Symposium on VLSI	Providence, RI, USA	16-18 May 2010	269 - 273
ieee	D	1	0	S.J. Piestrak	On Reducing Error Rate of Data Protected Using Systematic Unordered Codes in Asymmetric Channels	IEEE Euromicro Conference on Digital System Design: Architectures, Methods and Tools	Lille, France	1-3 Sept. 2010	133 - 140
ieee	D	1	0	J. Rajendran et al.	Memristor Based Programmable Threshold Logic Array	IEEE/ACM International Symposium on Nanoscale Architectures	Anaheim, CA, USA	17-18 Jun. 2010	5 - 10
PhD	D	1	0	H. Yan	Novel Nanowire Heterostructures for Nanoelectronic Applications (UMI 3435429)	Harvard University	Cambridge, MA, USA	11 May 2010	1 - 126
ieee	D	1	0	S. Aunet	On the Reliability of Ultra Low Voltage Circuits Built from Minority-3 Gates	IEEE European Conference on Circuit Theory and Design	Linköping, Sweden	29-31 Aug. 2011	540 - 543
Journal	A	8	8	A. Cilardo	Exploring the Potential of Threshold Logic for Cryptography-Related Operations	**IEEE Transactions on Computers**	Vol. 60, No. 4	Apr. 2011	452 - 462
Chp. 11	C	2	0	A.P.O. da Silva et al.	Adaptive Boolean Logic Using Ferroelectrics Capacitors as Basic Units of Artificial Neurons	Ferroelectrics - Applications	InTech	Aug. 2011	231 - 250
Journal	B	4	4	V. Erokhin and M.P. Fontana	Thin Film Electrochemical Memristive Systems for Bio-Inspired Computation	**Journal of Computational and Theoretical Nanoscience**	Vol. 8, No. 3	Mar. 2011	313 - 330
Journal	C	2	0	K.-J. Gan et al.	Design of Monostable–Bistable Transition Logic Element using the BiCMOS-based Negative Differential Resistance Circuit	**Analog Integrated Circuits and Signal Processing**	Vol. 68, No. 3	Sept. 2011	379 - 385
Journal	B	4	4	T. Gowda et al.	Identification of Threshold Functions and Synthesis of Threshold Networks	**IEEE Transactions on CAD of ICs and Systems**	Vol. 30, No. 5	May 2011	665 - 677
Journal	C	2	0	S.Kaya et al.	Improved Reconfigurability and Noise Margins in Threshold Logic Gates via Back-gate Biasing in DG-MOSFETs	**Analog Integrated Circuits and Signal Processing**	Vol. 68, No. 1	Jan. 2011	101 - 109
ICCAD-11	A	8	8	P.-Y. Kuo et al.	On Rewiring and Simplification for Canonicity in Threshold Logic Circuits	IEEE/ACM International Conference on Computer-Aided Design	San Jose, CA, USA	7-10 Nov. 2011	396 - 403
ieee	D	1	0	P. Shabadi et al.	Spin Wave Functions Nanofabric Update	IEEE/ACM International Symposium on Nanoscale Architectures	San Diego, CA, USA	8-9 Jun. 2011	107 - 113
ieee	D	1	0	M. Stankovic et al.	Mapping Decision Diagrams for Multiple-Valued Logic Functions into Threshold Logic Networks	IEEE International Symposium on Multiple-Valued Logic	Tuusula, Finland	23-25 May 2011	111 - 116
springer	D	1	0	G. Tufte	Metamorphosis and Artificial Development: An Abstract Approach to Functionality	In G. Kampis et al. (eds.): Advances in Artificial Life: Darwin Meets von Neumann	Springer LNCS 5777	8-12 Aug. 2011	83 - 90
Journal	C	2	0	Y. Wei and J. Shen	Novel Universal Threshold Logic Gate Based on RTD and Its Application	**Microelectronics Journal**	Vol. 42, No. 6	Jun. 2011	851 - 854
Journal	C	2	0	Y. Wei and J. Shen	Research of Logic Function Synthesis Algorithm Based on Threshold Logic	**Journal of Electronics & Information Technology**	Vol. 33, No. 7	Jul. 2011	1775 - 1778
Journal	A	8	8	J. Borresen and S. Lynch	Oscilatory Threshold Logic	**PLoS ONE**	Vol. 7, No. 11	Nov. 2012	e48498 (1 - 10)
ieee	D	1	0	C.H. Dara et al.	Delay Analysis for N-Input Current Mode Threshold Logic Gate	IEEE Computer Society Annual Symposium on VSLI	Amherst, MA, USA	19-21 Aug. 2012	344 - 349
ProQuest	D	1	0	N.K. Dixit and V. Kumari	A XOR Threshold Logic Implementation Through Resonant Tunneling Diode	**International Journal of VLSI Design & Communication Systems**	Vol.3, No.5	Oct. 2012	137 - 146
PhD	D	1	0	T.L. Gowda	Threshold Logic Properties and Methods: Applications to Post-CMOS Design Automation and Gene Regulation Modeling (UMI 3505795)	Arizona State University	Tempe, AZ, USA	May 2012	1 - 194
US 8,181,133	D	1	0	T.L. Gowda and S. Vrudhula	Combinational Equivalence Checking for Threshold Logic Circuits	Arizona State University	Washington, DC, USA	14 May 2012	1 - 24

ICCAD-12	**A**	**8**	**8**	N. Kulkarni et al.	Minimizing Area and Power of Sequential CMOS Circuits Using Threshold Decomposition	IEEE/ACM International Conference on Computer-Aided Design	San Jose, CA, USA	5-8 Nov. 2012	605 - 612
US 8,164,359	**D**	**1**	**0**	S. Leshner and S. Vrudhula	Threshold Logic Element Having Low Leakage Power and High Performance	Arizona State University	Washington, DC, USA	24 Apr. 2012	1 - 18
PhD	**D**	**1**	**0**	H. Manem	Design Approaches for Nanoscale Logic and Memory Architectures (UMI 3498598)	Polytehnic Institute of New York University	New York, NY, USA	Jan. 2012	1 - 111
Journal	**A**	**8**	**8**	H. Manem et al.	Stochastic Gradient Descent Inspired Training Technique for a CMOS/Nano Memristive Trainable Threshold Gate Array	**IEEE Transactions on Circuits and Systems I**	Vol. 59, No. 5	May 2012	1051 - 1060
ieee	**D**	**1**	**0**	N.S. Nukala et al.	Spintronic Threshold Logic Array (STLA) - A Compact, Low Leakage, Non-volatile Gate Array Architecture	IEEE/ACM International Symposium on Nanoscale Architectures	Amsterdam, The Netherlands	4-6 Jul. 2012	188 - 195
acm	**D**	**1**	**0**	A.K. Palaniswamy and S. Tragoudas	A Scalable Threshold Logic Synthesis Method Using ZBDDs	ACM Great Lakes Symposium on VLSI	Utah, USA	3-4 May 2012	307 - 310
Journal	**B**	**4**	**4**	A.K. Palaniswamy and S. Tragoudas	An Efficient Heuristic to Identify Threshold Logic Functions	**ACM Journal on Emerging Technologies in Computing**	Vol. 8, No. 3	Aug. 2012	19 (1 - 17)
Journal	**A**	**8**	**8**	J. Rajendran et al.	An Energy-Efficient Memristive Threshold Logic Circuit	**IEEE Transactions on Computers**	Vol. 61, No. 4	Apr. 2012	474 - 487
Journal	**A**	**8**	**8**	G.C. Rose et al.	Leveraging Memristive Systems in the Construction of Digital Logic Circuits (Invited)	**Proceedings of the IEEE**	Vol. 100, No. 6	Jun. 2012	2033 - 2049
CNNA-12	**C**	**2**	**0**	T. Shibata et al.	CMOS Supporting Circuitries for Nano-Oscillator-Based Associative Memories	International Workshop on Cellular Nanoscale Networks and Their Applications	Turin, Italy	29-31 Aug. 2012	1 - 5
PhD	**D**	**1**	**0**	Y. Sun	Computer Architectures Using Nanotechnology (UMI 3493764)	Lehigh University	Bethlehem, PA, USA	Jan. 2012	1 - 104
ieee	**D**	**1**	**0**	T. Tran et al.	Reconfigurable Threshold Logic Gates Using Memristive Devices	IEEE Subthreshold Microelectronics Conference	Waltham, MA, USA	9-10 Oct. 2012	art. 6404301 (1 - 3)
Journal	**D**	**1**	**0**	R.-S. Wei et al.	Reconfigurable Threshold Logic Element with SET and MOS Transistors	**Chinese Physics Letters**	Vol. 29, No. 2	Feb. 2012	028502 (1 - 5)
Journal	**C**	**2**	**0**	F. Xia et al.	Towards Power-Elastic Systems through Concurrency Management	**IET Computers and Digital Techniques**	Vol. 6, No. 1	Jan. 2012	33 - 42
Journal	**A**	**8**	**8**	V. Annampedu and M.D. Wagh	Decomposition of Threshold Functions into Bounded Fan-in Threshold Functions	**Information and Computation**	Vol. 227	Jun. 2013	84 - 101
Book	**B**	**4**	**4**	E. Dubrova	Fault-Tolerant Design	Springer	New York, NY	2013	1 - 185
ieee	**D**	**1**	**0**	F. Ercan and A. Muhtaroğlu	Energy-Delay Performance of Capacitive Threshold Logic (CTL) Circuits for Threshold Detection	IEEE International Conference on Energy Aware Computing Systems and Applications	Istanbul, Turkey	Dec. 2013	109 - 114
Journal	**A**	**8**	**8**	L. Gao et al.	Programmable CMOS/Memristor Threshold Logic	**IEEE Transactions on Nanotechnology**	Vol. 12, No. 2	Mar. 2013	115 - 119
US 8,601,417	**D**	**1**	**0**	T. Gowda and S. Vrudhula	Decomposition Based Approach for the Synthesis of Threshold Logic Circuits	Arizona State University	Washington, DC, USA	Dec. 2013	1 - 34
Journal	**C**	**2**	**0**	M. Maleknejad et al.	New CNTFET-Based Arithmetic Cells with Weighted Inputs for High Performance Energy Efficient Applications	**IEICE Transactions on Electronics**	Vol. E96-C, No. 7	Jul. 2013	1019 - 1027
ieee	**D**	**1**	**0**	A. Neutzling et al.	Synthesis of Threshold Logic Gates to Nanoelectronics	IEEE Symposium on Integrated Circuits and Systems Design	Curitiba, Brazil	Sept. 2013	6644871 (1 - 6)

Journal	**A**	**8**	**8**	M.D. Pickett and R.S. Williams	Phase Transitions Enable Computational Universality in Neuristor-based Cellular Automata	**Nanotechnology**	Vol. 24, No. 38	Sept. 2013	art. 384002 (1 - 7)
Journal	**C**	**2**	**0**	A. Rothenbuhler et al.	Reconfigurable Threshold Logic Gates using Memristive Devices	**Journal of Low Power Electronics and Applications**	Vol. 3, No. 2	May 2013	174 - 193
ICCAD-13	**A**	**8**	**8**	C.K. Tsai et al.	Sensitization Criterion for Threshold Logic Circuits and its Application	IEEE/ACM International Conference on Computer-Aided Design	San Jose, CA, USA	Nov. 2013	226 - 233
Journal	**B**	**4**	**4**	A.P. James et al.	Resistive Threshold Logic	**IEEE Transactions on VLSI Systems**	Vol. 22, No. 1	Jan. 2014	190 - 195
Journal	**C**	**2**	**0**	A. Kotsialos	Logic Gate and Circuit Training on Randomly Dispersed Carbon Nanotubes	**International Journal of Unconventional Computing**	Vol. 10, No. 5-6	2014	473 - 497
ieee	**D**	**1**	**0**	N. Kulkarni et al.	A fast, energy efficient, field programmable threshold-logic array	IEEE International Conference on Field-Programmable Technology (FPT)	Shanghai, China	10-12 Dec. 2014	300 - 305
ieee	**D**	**1**	**0**	H. Li et al.	Emerging Memristor Technology Enabled Next Generation Cortical Processor	IEEE International System-on-Chip Conference (SOCC)	Las Vegas, NV, USA	2-5 Sept. 2014	377 - 382
ieee	**D**	**1**	**0**	H. Li et al.	Neuromorphic hardware acceleration enabled by emerging technologies (Invited paper)	IEEE International Symposium on Integrated Circuits (ISIC)	Singapore	10-12 Dec. 2014	124 - 127
DATE-14	**B**	**4**	**4**	C.-C. Lin	Rewiring for Threshold Logic Circuit Minimization	International Design, Automation and Test in Europe Conference and Exhibition	Dresden, Germany	Mar. 2014	6800335 (1 - 6)
ISCAS-14	**C**	**2**	**0**	A. Neutzling et al.	A Constructive Approach for Threshold Logic Circuit Synthesis	IEEE International Symposium on Circuits & Systems (ISCAS)	Melbourne, Australia	Jun. 2014	385 - 388
Journal	**B**	**4**	**4**	N.S. Nukala et al.	Spintronic Threshold Logic Array (STLA) - A Compact, Low Leakage, Non-volatile Gate Array Architecture	**Journal of Parallel and Distributed Computing**	Vol. 74, No. 6	Jun. 2014	2452 - 2460
europment	**D**	**1**	**0**	A.I. Prangishvili et al.	Two Methods of Obtaining a Minimal Upper Estimate for the Error Probability of the Restoring Formal Neuron	International Conference on Mathematical Methods, Mathematical Models and Simulation in Science and Engineering	Interlaken, Switzerland	Feb. 2014	37 - 41
Journal	**B**	**4**	**4**	M. Stankovic et al.	Threshold Logic Realization of Discrete Functions through Heterogeneous Decision Diagrams	**Journal of Multiple-Valued Logic & Soft Computing**	Vol. 23, No. 3-4	2014	315 - 335
US 8,832,614	**D**	**1**	**0**	S. Vrudhula and N. Kulkarni	Technology Mapping for Threshold and Logic Gate Hybrid Circuits	Arizona State University	Washington, DC, USA	9 Sept. 2014	1 - 27
NanoArch-14	**D**	**1**	**0**	J. Yang et al.	Integration of Threshold Logic Gates with RRAM Devices for Energy Efficient and Robust Operation	IEEE/ACM International Symposium on Nanoscale Architectures (NanoArch)	Paris, France	8-10 Jul. 2014	39 - 44
IJCNN-14	**A**	**8**	**8**	Y. Zhang et al.	Implementation of Memristive Neural Networks with Spike-Rate-Dependent Plasticity Synapses	IEEE International Joint Conference on Neural Networks (IJCNN)	Beijing, China	6-11 Jul. 2014	2226 - 2233
Journal	**A**	**8**	**8**	A.M. Burke	InAs Nanowire Transistors with Multiple, Independent Wrap-Gate Segments	**Nano Letters**	Vol. 15, No. 5	Apr. 2015	2836 - 2843
ingentaconnect	**D**	**1**	**0**	A.P.O. da Silva et al.	Adaptive Boolean Logic Using Ferroelectrics Capacitors as Basic Units of Artificial Neurons and Its Implementation in FPGA	**Integrated Ferroelectrics**	Vol. 159, No. 1	Jun. 2015	23 - 33
ieee	**D**	**1**	**0**	F. Ercan and A. Muhtaroglu	Comparative power-delay performance analysis of threshold logic technologies	IEEE International Conference on Energy Aware Computing Systems & Applications (ICEAC)	Cairo, Egypt	24-26 Mar. 2015	7352166 (1 - 4)
Journal	**B**	**4**	**4**	A.P. James et al.	Threshold Logic Computing: Memristive-CMOS Circuits for Fast Fourier Transform and Vedic Multiplication	**IEEE Transactions on Very Large Scale Integration (VLSI) Systems**	Vol. 23, No. 11	Nov. 2015	2690 - 2694
ieee	**D**	**1**	**0**	S.R.S. Klavakolanu et al.	A review report on low power VLSI systems analysis and modeling techniques	IEEE International Conference on Signal Processing And Communication Engineering Systems (SPACES)	Guntur, India	2-3 Jan. 2015	142 - 146
ieee	**D**	**1**	**0**	D. Mahalanabis et al.	A Nonvolatile Sense Amplifier Flip-Flop Using Programmable Metallization Cells	**IEEE Journal on Emerging and Selected Topics in Circuits and Systems**	Vol. 5, No. 2	Jun. 2015	2015 - 2013

PhD	**D**	**1**	**0**	D. Mahalanabis	Multilevel Resistance Programming in Conductive Bridge Resistive Memory	Arizona State University	Tempe, AZ, USA	Dec. 2015	1 - 146
ICCAD-15	**A**	**8**	**8**	A. Neutzling et al.	Threshold Logic Synthesis Based on Cut Pruning	IEEE/ACM International Conference on Computer-Aided Design	Austin, TX, USA	2-6 Nov. 2015	494 - 499
ASPLOS-15	**A**	**8**	**8**	J. Pang et al.	More is Less, Less is More: Molecular-Scale Photonic NoC Power Topologies	International Conference on Architectural Support for Programming Languages and Operating Systems	Istanbul, Turkey	14-18 Mar. 2015	283 - 296
Chp. 18	**B**	**4**	**4**	U. Ruckert	Brain-Inspired Architectures for Nanoelectronics	**CHIPS 2020, vol. 2: New Vistas in Nanoelectronics**	Springer	2016	249 - 274
Chp. 4	**B**	**4**	**4**	I. Vourkas & G.C. Sirakoulis	Memristor-Based Logic Circuits	**Memristor-Based Nanoelectronic Computing Circuits and Architectures**	Springer	Aug. 2015	61 - 100
ISCAS-15	**C**	**2**	**0**	S. Vrudhula	Design of Threshold Logic Gates using Emerging Devices	IEEE International Symposium on Circuits and Systems (ISCAS)	Lisbon, Portugal	24-27 May 2015	373 - 376
ISCAS-15	**C**	**2**	**0**	J. Yang et al.	Fast and Robust Differential Flipflops and Their Extension to Multi-input Threshold Gates	IEEE International Symposium on Circuits and Systems (ISCAS)	Lisbon, Portugal	24-27 May 2015	822 - 825
ieee	**D**	**1**	**0**	J. Yang et al.	Dynamic and Leakage Power Reduction of ASICs Using Configurable Threshold Logic Gates	IEEE Custom Integrated Circuits Conference (CICC)	San Jose, CA,USA	28-30 Sept. 2015	7338369 (1 - 4)
ProQuest	**D**	**1**	**0**	M. Yao et al.	Function Synthesis Algorithm of RTD-based Universal Threshold Logic Gate	**Journal of Applied Mathematics**	Vol. 2015	2015	art. 827572
springer	**D**	**1**	**0**	M. Yao et al.	Design of a Novel RTD-based Three-variable Universal Logic Gate	**Frontiers of Information Technology & Electronic Engineering**	Vol. 16, No. 8	Aug. 2015	694 - 699
Journal	**B**	**4**	**4**	C.B. Dara et al.	Delay Analysis for Current Mode Threshold Logic Gate Designs	**IEEE Transactions on Very Large Scale Integration (VLSI) Systems**	Vol. PP, No. 99	4 Oct. 2016	1 - 9
Book	**B**	**4**	**4**	I.N. da Silva et al.	Artificial Neural Networks -- A Practical Course	Springer ISBN: 978-3-319-43161-1 (Print) 978-3-319-43162-8 (Online)	Springer	2017	http://www.springer.com/gp/book/9783319431611
acm	**D**	**1**	**0**	D. Fan	Ultra-Low Energy Reconfigurable Spintronic Threshold Logic Gate	Proceedings of the Great Lakes Symposium on VLSI (GLSVLSI)	Boston, MA, USA	18-20 May 2016	385 - 388
arXiv	**D**	**1**	**0**	J. Freixas et al.	Characterization of Threshold Functions: State of the Art, Some New Contributions and Open Problems	arXiv.org > cs.GT > arXiv:1603.00329v1	arXiv	Mar. 2016	1 - 23
Book	**A**	**8**	**8**	I. Goodfellow et al.	Deep Learning	MIT Press	Boston, MA, USA	2016	http://www.deeplearningbook.org/
ieee	**D**	**1**	**0**	Z. He and D. Fan	Energy Efficient Reconfigurable Threshold Logic Circuit with Spintronic Devices	**IEEE Transactions on Emerging Topics in Computing**	Vol. PP, No. 99	9 Dec. 2016	1 - 14
ARITH-16	**C**	**2**	**0**	G. Jaberipur et al.	A Formulation of Fast Carry Chains Suitable for Efficient Implementation with Majority Elements	IEEE Symposium on Computer Arithmetic	Santa Clara, CA, USA	10-13 Jul. 2016	8 - 15
Journal	**B**	**4**	**4**	N. Kulkarni et al.	Reducing Power, Leakage, and Area of Standard-Cell ASICs Using Threshold Logic Flip-Flops	**IEEE Transactions on Very Large Scale Integration (VLSI) Systems**	Vol. 24, No. 9	Sept. 2016	2873 - 2886
arXiv	**D**	**1**	**0**	D. Kumar et al.	On Fault-Tolerant Design of Exclusive-OR Gates in QCA	arXiv.org > cs.ET > arXiv:1612.02975v1	arXiv	Dec. 2016	1 - 10
ICCAD-16	**A**	**8**	**8**	N.-Z. Lee et al.	Analytic approaches to the collapse operation and equivalence verification of threshold logic circuits	International Conference on Computer-Aided Design	Austin, TX, USA	7-10 Nov. 2016	art. 5 (http://dl.acm.org/citation.cfm?id=2967001)
ieee	**D**	**1**	**0**	C.-Y. Lin et al.	Minimization of Number of Neurons in Voronoi Diagram-based Artificial Neural Networks	**IEEE Transactions on Multi-Scale Computing Systems**	Vol. 2, No. 4	Oct. - Dec. 2016	225 - 233
Journal	**A**	**8**	**8**	A.K. Maan et al.	A Survey of Memristive Threshold Logic Circuits	**IEEE Transactions on Neural Networks and Learning Systems**	Vol. PP, No. 99	3 May 2016	1 - 13

	Journal	**A**	**8**	**8**		I. Vourkas and G.Ch. Sirakoulis	Emerging Memristor-Based Logic Circuit Design Approaches: A Review	**IEEE Circuits and Systems Magazine**	Vol. 16, No. 3	Aug. 2016	15 - 30
	Wiki article	**D**	**1**	**0**		***	C-element	https://en.wikipedia.org/wiki/C-element	web	Sept. 2016	
495.00			**495**	**368**	**368.00**						

J015	**Journal**					**S. Roy, and V. Beiu**	**Majority Multiplexing — Economical Redundant Fault-Tolerant Design for Nano Architectures**	**IEEE Transactions on Nanotechnology**	**vol. 4, no. 4**	**Jul. 2005**	**441 - 451**
	CiteSeerX	**D**	**1**	**0**		D. Bhaduri and S. Shukla	Comparing Reliability/Redundancy Trade-offs of Von Neumann Based Multiplexing Architectures	Virginia Polytehnic Institute and State University	Blacksburg, USA	Jan. 2004	1 - 21
	Chp. 6	**B**	**4**	**4**		D. Bhaduri and S. Shukla	Tools and Techniques for Evaluating Reliability Trade-offs for Nano-Architectures	Chapter 6 in S. Shukla and I. Bahar (Eds.): "Nano, Quantum and Molecular Computing: Implications to High Level Design and Validation"	Springer	May 2004	157 - 211
	ieee	**D**	**1**	**0**		D. Bhaduri and S. Shukla	Reliability Evaluation of von Neumann Multiplexing Based Defect-tolerant Majority Circuits	IEEE International Conference on Nanotechnology	Munich, Germany	16-19 Aug. 2004	599 - 601
	lanl.gov	**D**	**1**	**0**		D. Bhaduri et al.	Reliability/Redundancy Trade-off Evaluation for Multiplexed Architectures Used to Implement Quantum Dot Based Computing	Los Alamos National Laboratory LA-UR-04-4882	DOE, USA	2004	1 - 15
	PhD	**D**	**1**	**0**		J. Han	Fault-tolerant Architectures for Nanoelectronic and Quantum Devices	Technical University of Delft	Delft, Netherlands	30 Nov. 2004	1 - 151
	Journal	**A**	**8**	**8**		J. Han et al.	Toward Hardware-Redundant, Fault-Tolerant Logic for Nanoelectronics	**IEEE Design and Test of Computers**	Vol. 22, No. 4	Jul.-Aug. 2005	328 - 339
	Chp. 17	**B**	**4**	**4**		K.K. Likharev and D.B. Strukov	CMOL: Devices, Circuits, and Architectures	In G. Cuniberti, G. Fagas, and K. Richter (Eds.): "Introducing Molecular Electronics" (LNP 680)	Springer	Dec. 2005	447 - 477
	Journal	**A**	**8**	**8**		D.B. Strukov and K.K. Likharev	CMOL FPGA: A Reconfigurable Architecture for Hybrid Digital Circuits with Two-Terminal Nanodevices	**Nanotechnology**	Vol. 16	Apr. 2005	888 - 900
	lanl.gov	**D**	**1**	**0**		D. Badhuri and S. Shukla	Reliability/Redundancy Trade-off Evaluation for Multiplexed Architectures Used to Implement Quantum Dot Based Computing	Los Alamos Unrestricted Report LA-UR-05-4882	Los Alamos, NM, USA	2006	1 - 15
	lanl.gov	**D**	**1**	**0**		D. Badhuri et al.	A Hybrid Framework for Design and Analysis of Fault-tolerant Architectures for Nanoscale Molecular Crossbar Memories	Los Alamos Unrestricted Report LA-UR-05-7196	Los Alamos, NM, USA	2006	1 - 7
	ieee	**D**	**1**	**0**		D. Badhuri et al.	Methods and Tools for Reliability Driven Defect- and Fault-Tolerant Design of Nanosystems	IEEE International Conference on Nanotechnology	Cincinnati, OH, USA	16-20 Jul. 2006	359 - 362
	WCCI-06	**A**	**8**	**8**		R. Eickhoff et al.	SIRENS: A Simple Reconfigurable Neural Hardware Structure for Artificial Neural Network Implementations	IEEE World Congress on Computational Intelligence	Vancouver, Canada	16-21 Jul. 2006	2830 - 2837
	GLOBECOM-06	**B**	**4**	**4**		M. Ivkovic et al.	Construction of Memory Circuits Using Unreliable Components Based on Low-Density Parity-Check Codes	IEEE Global Telecommunications Conference	San Francisco, CA, USA	27 Nov. - 1 Dec. 2006	1 - 5
	ieee	**D**	**1**	**0**		F. Martorell and A. Rubio	Defect and Fault Tolerant Cell Architecture for Feasible Nanoelectronic Designs	IEEE International Conference on Design and Test of Integrated Systems in Nanoscale Technology	Tunis, Tunisia	5-7 Sept. 2006	244 - 249
	ieee	**D**	**1**	**0**		A. Namazi et al.	Reliable Interconnect Grid for Ultra Deep Submicron	IEEE Dallas/CAS Workshop on Design, Applications, Integration and Software	Richardson, TX, USA	29-30 Oct. 2006	107 - 110
	PhD	**D**	**1**	**0**		G.R. Roelke	Fault and Defect Tolerant Computer Architectures: Reliable Computing With Unreliable Devices	Air Force Institute of Technology	Wright-Patterson, OH, USA	Sept. 2006	1 - 421
	PhD	**D**	**1**	**0**		J. Sima	Neuronové Síte Jako Modely Analogových Výpoctu	Academy of the Czech Republic	Prague, Czech Republic	Apr. 2006	1 - 46

PhD	**D**	**1**	**0**	D.B. Strukov	Digital Architectures for Hybrid CMOS/Nanodevice Circuits	Stony Brook University	Stony Brook, NY, USA	Aug. 2006	1 - 128
ieee	**D**	**1**	**0**	E.R. Taylor et al.	An Investigation into the Maximum Tolerable Error Rate of Majority Gates for Reliable Computation	ACM/IEEE International Conference on Nano Architectures	Boston, MA, USA	17 Jun. 2006	1 - 8
PhD	**D**	**1**	**0**	D. Bhaduri	Design and Analysis of Defect- and Fault-Tolerant Nano-Computing Systems	Virginia Polytechnic Institute and State University	Blacksburg, VA, USA	19 Feb. 2007	1 - 232
Journal	**A**	**8**	**8**	D. Bhaduri et al.	Comparing Reliability-Redundancy Tradeoffs for Two von Neumann Multiplexing Architectures	**IEEE Transactions on Nanotechnology**	Vol. 6, No. 3	May 2007	265 - 279
Journal	**A**	**8**	**8**	D. Bhaduri et al.	Reliability Analysis of Large Circuits Using Scalable Techniques and Tools	**IEEE Transactions on Circuits and Systems I**	Vol. 54, No. 11	Nov. 2007	2447 - 2460
ieee	**D**	**1**	**0**	P. Bharkhada and C. Chen	On the Behaviors of Multi-island Structure for Single-Electron Threshold Logic Circuits	IEEE International Conference on Nanotechnology	Hong Kong, China	2-5 Aug. 2007	66 - 69
ieee	**D**	**1**	**0**	C. Chen and F. Zhou	Towards Reliability Improvement for Nanoelectronic Circuits Using Gate Replication	IEEE International Conference on Nanotechnology	Hong Kong, China	2-5 Aug. 2007	597 - 600
Journal	**A**	**8**	**8**	C. Chen	Reliability-Driven Gate Replication for Nanometer-Scale Digital Logic	**IEEE Transactions on Nanotechnology**	Vol. 6, No. 3	May 2007	303 - 308
PhD	**D**	**1**	**0**	R. Eickhoff	Fehlertolerante Neuronale Netze zur Approximation von	University of Paderborn	Paderborn,	11 Jul. 2007	1 - 260
dblp	**D**	**1**	**0**	M.M. Eshaghian-	Parallel and Fault-Tolerant Routing in Nanoscale Spin-Wave	International Conference on Computer Design CDES-07 (World	Las Vegas, NV,	25-28 Jun.	3 - 9
Journal	**B**	**4**	**4**	S.-L. Jeng et al.	A Review of Reliability Research on Nanotechnology	**IEEE Transactions on Reliability**	Vol. 56, No. 3	Sept. 2007	401 - 410
acm	**D**	**1**	**0**	K.	Probabilistic Maximum Error Modeling for Unreliable Logic	ACM International Great Lakes Symposium on VLSI	Stresa, Italy	11-13 Mar.	223 - 226
ieee	**D**	**1**	**0**	K. Lingasubramanian and S. Bhanja	Probabilistic Error Modeling for Sequential Logic	IEEE International Conference on Nanotechnology	Hong Kong, China	2-5 Aug. 2007	616 - 620
arXiv	**D**	**1**	**0**	F. Martorell and A. Rubio	Cell Architecture for Nanoelectronic Design	European Nano Systems (co-located with the 2nd Workshop on Nano Technology Transfer in Europe) -- 14-15 Dec. 2006	Paris, France	10 Aug. 2007	114 - 119
PhD	**D**	**1**	**0**	H. Naeimi	Reliable Integration of Terascale Systems with Nanoscale Devices	California Institute of Tecnology	Pasadena, CA, USA	4 Sept. 2007	1 - 181
ieee	**D**	**1**	**0**	A. Namazi and M. Nourani	Distributed Voting for Fault-Tolerant Nanoscale Systems	IEEE International Conference on Computer Design	Lake Tahoe, CA, USA	7-10 Oct. 2007	568 - 573
ieee	**D**	**1**	**0**	A. Namazi et al.	Reliability Analysis and Distributed Voting for NMR Nanoscale Systems	IEEE International Design and Test Workshop	Cairo, Egypt	16-18 Dec. 2007	130 - 135
PhD	**D**	**1**	**0**	S. Navab	Parallel Computing with Spin Waves on Nano-scale Integrated Circuits (UMI 3272261)	University of California Los Angeles	Los Angeles, CA, USA	2007	1 - 170
Journal	**A**	**8**	**8**	G.R. Roelke at al.	Analytical Models for the Performance of von Neumann Multiplexing	**IEEE Transactions on Nanotechnology**	Vol. 6, No. 1	Jan. 2007	75 - 89
Journal	**B**	**4**	**4**	G.R. Roelke at al.	A Cache Architecture for Extremely Unreliable Nanotechnologies	**IEEE Transactions on Reliability**	Vol. 56, No. 2	Jun. 2007	182 - 197
acm	**D**	**1**	**0**	M.H. Sulieman	Reliability of single-electron logic gates	ACM Conference on Microelectronics, Nanoelectronics, Optoelectronics	Istanbul, Turkey	27-29 May 2007	50 - 53
Journal	**A**	**8**	**8**	B. Vasic and S.K. Chilappagari	An Information Theoretical Framework for Analysis and Design of Nanoscale Fault-Tolerant Memories Based on Low-Density Parity-Check Codes	**IEEE Transactions on Circuits and Systems I**	Vol. 54, No. 11	Nov. 2007	2438 - 2446
Journal	**A**	**8**	**8**	C. Chen and Y. Mao	A Statistical Reliability Model for Single-Electron Threshold Logic	**IEEE Transactions on Electron Devices**	Vol. 55, No. 6	Jun. 2008	1547 - 1553
ieee	**D**	**1**	**0**	T.J. Dysart and P.M. Kogge	System Reliabilities when Using Triple Modular Redundancy in Quantum-Dot Cellular Automata	IEEE International Symposium on Defect and Fault Tolerance of VLSI Systems	Cambridge, MA, USA	1-3 Oct. 2008	72 - 80

Journal	**C**	**2**	**0**	K.K. Likharev et al.	Hybrid CMOS/Nanoelectronic Circuits: Opportunities and Challenges	**Journal of Nanoelectronics and Optoelectronics**	Vol. 3, No. 3	Dec. 2008	203 - 230
Journal	**C**	**2**	**0**	E. Lughofer and C. Guardiola	On-line Fault Detection with Data-Driven Evolving Fuzzy Models	**Control and Intelligent Systems**	Vol. 36, No. 4	2008	307 - 317
PhD	**D**	**1**	**0**	X. Ma	Physical/Biochemical Inspired Computing Models for Reliable Nano-technology Systems	**Northeastern University**	Boston, MA, USA	Nov. 2008	1 - 277
ieee	**D**	**1**	**0**	X. Ma and F. Lombardi	Fault Tolerant Schemes for QCA Systems	IEEE International Symposium on Defect and Fault Tolerance of VLSI Systems	Cambridge, MA, USA	1-3 Oct. 2008	236 - 244
Journal	**C**	**2**	**0**	F. Martorell and A. Rubio	Cell Architecture for Nanoelectronic Design	**Microelectronics Journal**	Vol. 39, No. 8	Aug. 2008	1041 - 1050
PhD	**D**	**1**	**0**	H. Naeimi	Reliable Integration of Terascale Systems with Nanoscale Devices (UMI 3526020)	California Institute of Technology	Pasadena, CA, USA	24 Jan. 2008	1 - 172
Journal	**A**	**8**	**8**	H. Naeimi and A. DeHon	Fault-tolerant Sub-litographic Design with Rollback Recovery	**Nanotechnology**	Vol. 19, No. 11	19 Mar. 2008	115708 (1 - 17)
ieee	**D**	**1**	**0**	A. Namazi et al.	Highly Reliable A/D Converter using Analog Voting	IEEE International Conference on Computer Design	Lake Tahoe, CA, USA	12-15 Oct. 2008	334 - 339
ieee	**D**	**1**	**0**	A. Namazi et al.	A voterless strategy for defect-tolerant nano-architectures	ACM/IEEE International Conference on Nano Architectures	Anaheim, CA, USA	12-13 Jun. 2008	38 - 45
ISCAS-08	**C**	**2**	**0**	V. Puthucode and C. Chen	An Experimental Study on Multi-Island Structures for Single-Electron Tunneling Based Threshold Logic	IEEE International Symposium on Circuits and Systems	Seattle, WA, USA	18-21 May 2008	600 - 603
ieee	**D**	**1**	**0**	A. Shareef et al.	Selective Redundancy: Evaluation of Temporal Reliability Enhancement Scheme for Nanoelectronic Circuits	IEEE International Conference on Nanotechnology	Arlington, TX, USA	18-21 Aug. 2008	895 - 898
Journal	**A**	**8**	**8**	M. Stanisavljevic et al.	Optimization of Nanoelectronic Systems' Reliability under Massive Defect Density using Cascaded R-fold Modular Redundancy	**Nanotechnology**	Vol. 19, No. 46	19 Nov. 2008	465202 (1 - 9)
Chp. 4	**B**	**4**	**4**	D.B. Strukov	Hybrid Semiconductor-Molecular Integrated Circuits for Digital Electronics: CMOL Approach	In A. Korkin and F. Rosei (Eds.): Nanoelectronics and Photonics -- From Atoms to Materials, Devices, and Architectures	Springer	Sept. 2008	15 - 57
Chp. 10	**B**	**4**	**4**	S. Ahuja et al.	Fault and Defect Tolerant Architectures for Nano-Computing	In M.M. Eshaghian-Wilner (Ed.): "Bio-Inspired and Nanoscale Integrated Computing"	Wiley-VCH	Jun. 2009	263 - 294
IDT-09	**D**	**1**	**0**	S. Askari et al.	Scalable Mean Voting Mechanism for Fault Tolerant Analog Circuits	IEEE International Design and Test Workshop	Riyadh, Saudi Arabia	5-17 Nov. 2009	5404145 (1 - 6)
ieee	**D**	**1**	**0**	S. Aunet	Subthreshold Minority-3 Gates and Inverters Used for 32-bit Serial and Parallel Adders Implemented in 90 nm CMOS	IEEE Norchip International Conference	Trondheim, Norway	16-17 Nov. 2009	5397845 (1 - 6)
ieee	**D**	**1**	**0**	J.H. Collet et al.	Comparison of Fault-Tolerance Techniques for Massively Defective Fine- and Coarse-Grained Nanochips	IEEE International Conference on Mixed Design of Integrated Circuits and Systems	Lodz, Poland	25-27 Jun. 2009	23 - 30
PhD	**D**	**1**	**0**	T.J. Dysart	It's All About the Signal Routing: Understanding the Reliability of QCA Circuits and Systems	**Notre Dame University**	Notre Dame, IN, USA	Jul. 2009	1 - 135
Journal	**B**	**4**	**4**	T.J. Dysart and P.M. Kogge	Analyzing the Inherent Reliability of Moderately Sized Magnetic and Electrostatic QCA Circuits Via Probabilistic Transfer Matrices	**IEEE Transactions on VLSI Systems**	Vol. 17, No. 4	Apr. 2009	507 - 516
Chp. 8	**B**	**4**	**4**	M.M. Eshaghian-Wilner and S. Navab	Parallel Computing with Spin Waves	In M.M. Eshaghian-Wilner (Ed.): "Bio-Inspired and Nanoscale Integrated Computing"	Wiley-VCH	Jun. 2009	225 - 242
ieee	**D**	**1**	**0**	K. Lingasubramanian and S. Bhanja	An Error Model to Study the Behavior of Transient Errors in Sequential Circuits	IEEE International Conference on VLSI Design	New Delhi, India	5-9 Jan. 2009	485 - 490

arXiv	D	1	0	K. Lingasubramanian et al.	Naximum Error Modeling for Fault-Tolerant Computation using Maximum a posteriori (MAP) Hypothesis	https://arxiv.org/abs/0906.3282		27 Oct. 2009	1 - 14
ieee	D	1	0	M.H. Sulieman	Threshold-Voltage Variations Effects on the Reliability of Nano-scale CMOS Logic Gates	IEEE Nanotechnology Conference	Genoa, Italy	26-30 Jul. 2009	744 - 747
springer	D	1	0	M.H. Sulieman	On the Reliability of Interconnected CMOS Gates Considering MOSFET Threshold-Voltage Variations	International Conference on Nano-Networks (Springer LNICST 20)	Luzern, Switzerland	18-20 Oct. 2009	251 - 258
PhD	D	1	0	S. Wang	Reliable and High-Performance Architecture for Nanoscale Integrated Systems	University of Connecticut	Storrs, CT, USA	11 Sept. 2009	1 - 153
Journal	B	4	4	S. Wang et al.	Towards Achieving Reliable and High-performance Nanocomputing via Dynamic Redundancy Allocation	**ACM Journal on Emerging Technologies in Computing Systems**	Vol. 5, No. 1	Jan. 2009	2 (1 - 21)
ieee	D	1	0	Askari et al.	Scalable Mean Voter for Fault-Tolerant Mixed-Signal Circuits	IEEE Aerospace Conference	Big Sky, Montana, USA	6-13 Mar. 2010	1216 (1 - 10)
ieee	D	1	0	S. Aunet and A. Hasanbegovic	Memory Elements Based on Minority-3 Gates and Inverters Implemented in 90 nm CMOS	IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems	Vienna, Austria	14-16 Apr. 2010	267 - 272
ieee	D	1	0	T. Ban et al.	A Simple Fault-tolerant Digital Voter Circuit in TMR Nanoarchitectures	IEEE International NEWCAS Conference	Montreal, Canada	20-23 Jun. 2010	269 - 272
Journal	A	8	8	M. Haselman and S. Hauck	The Future of Integrated Circuits: A Survey of Nanoelectronics	**Proceedings of the IEEE**	Vol. 98, No. 1	Jan. 2010	11 - 38
Chp.	B	4	4	B. Joshi et al.	Fault Tolerant Nanocomputing	In C. Huang (ed.): Robust Computing with Nano-scale Devices	Springer LNEE 58	Mar. 2010	7 - 27
PhD	D	1	0	K. Lingasubramanian	Probabilistic Error Analysis Models for Nano-Domain VLSI Circuits (UMI 3424479)	University of South Florida	Tampa, FL, USA	3 Mar. 2010	1 - 114
Journal	B	4	4	A. Mukati	A Survey of Memory Error Correcting Techniques for Improved Reliability	**Journal of Network and Computer Applications**	Vol. 34, No. 2	Mar. 2010	517 - 522
PhD	D	1	0	A. Namazi	Design-for-Reliability Techniques for Nanometer VLSI (UMI 3414927)	University of Texas at Dallas	Dallas, TX, USA	May 2010	1 - 91
Journal	B	4	4	A. Namazi et al.	A Fault-Tolerant Interconnect Mechanism for NMR Nanoarchitectures	**IEEE Transactions on VLSI Systems**	Vol. 18, No. 10	Oct. 2010	1433 - 1446
Journal	B	4	4	A. Namazi and M. Nourani	Gate-Level Redundancy: A New Design-for-Reliability Paradigm for Nanotechnologies	**IEEE Transactions on VLSI Systems**	Vol. 18, No. 5	May 2010	775 - 786
PhD	D	1	0	S. Wang	Reliable and High-Performance Architecture for Nanoscale Integrated Systems (UMI 3451316)	University of Connecticut	Storrs, CT, U.S	2010	1 - 141
ieee	D	1	0	S. Askari and M. Nourani	Highly Reliable Analog Filter Design Using Analog Voting	IEEE Saudi International Electronics, Communications and Photonics Conference	Riyadh, Saudi Arabia	24-26 Apr. 2011	1 - 6
Journal	B	4	4	S. Askari et al.	Fault-tolerant A/D Converter using Analogue Voting	**IET Circuits, Devices & Systems**	Vol. 5, No. 6	Nov. 2011	462 - 470
ieee	D	1	0	I.I. Basith et al.	Performance Enhancement of Single Electron Junction 1-bit Full Adder	IEEE International Conference on Electronics, Circuits and Systems	Beirut, Lebanon	11-14 Dec. 2011	157 - 160
ISCAS-11	C	2	0	H.K.O. Berge and S. Aunet	Multi-Objective Optimization of Minority-3 Functions for Ultra-Low Voltage Supplies	IEEE International Symposium on Circuits and Systems	Rio de Janeiro, Brazil	15-18 May 2011	2313 - 2316
Journal	A	8	8	T.J. Dysart and P.M. Kogge	Reliability Impact of N-Modular Redundancy in QCA	**IEEE Transactions on Nanotechnology**	Vol. 10, No. 5	Sept. 2011	1015 - 1022
Journal	B	4	4	N.H. Hamid et al.	Probabilistic Neural Computing with Advanced Nanoscale MOSFETs	**Neurocomputing**	Vol. 74, No. 6	Feb. 2011	930 - 940
Journal	B	4	4	J. Han et al.	Reliability Evaluation of Logic Circuits using Probabilistic Gate Models	**Microelectronics Reliability**	Vol. 51, No. 2	Feb. 2011	468 - 476
Journal	A	8	8	J. Han et al.	On the Reliability of Computational Structures using Majority Logic	**IEEE Transactions on Nanotechnology**	Vol. 10, No. 5	Sep. 2011	1099 - 1112

Journal	**B**	**4**	**4**	K. Lingasubramanian et al.	Maximum Error Modeling for Fault-tolerant Computation using Maximum a posteriori (MAP) Hypothesis	**Microelectronics Reliability**	Vol. 51, No. 2	Feb. 2011	485 - 501
Journal	**B**	**4**	**4**	A. Mukati	A Survey of Memory Error Correcting Techniques for Improved Reliability	**Journal of Network and Computer Applications**	Vol. 34, No. 2	Mar. 2011	517 - 522
PhD	**D**	**1**	**0**	A.A. Saha	Stochastic Resonance in Nanoscale Systems	Department of Physics, University of Alberta	Edmonton, Alberta	2011	1 - 159
Journal	**B**	**4**	**4**	A.A. Saha and J.A. Tuszynski	Signal Transmission in Carbon Nanotube Arrays	**Journal of Computational and Theoretical Nanoscience**	Vol. 8, No. 1	Jan. 2011	60 - 68
Book	**B**	**4**	**4**	M. Stanisavljević et al.	Reliability of Nanoscale Circuits and Systems: Methodologies and Circuit Architectures	Springer	New York	2011	1 - 195
Journal	**D**	**1**	**0**	C. Yu	Accurate SER Estimation Based on Probabilistic Transform Matrix with Dynamic Ordering	**Advances in Information Sciences and Service Sciences**	Vol. 3, No. 3	Apr. 2011	109 - 114
Journal	**C**	**2**	**0**	M. Zhu et al.	New Mix Codes for Multiple Bit Upsets Mitigation in Fault-secure Memories	**Microelectronics Journal**	Vol. 42, No. 3	Mar. 2011	553 - 561
Journal	**B**	**4**	**4**	S. Askari and M. Nourani	Design Methodology for Mitigating Transient Errors in Analogue and Mixed-signal Circuits	**IET Circuits, Devices & Systems**	Vol. 6, No. 6	Nov. 2012	447 - 456
Journal	**A**	**8**	**8**	N. Aymerich et al.	Adaptive Fault-Tolerant Architecture for Unreliable Technologies with Heterogeneous Variability	**IEEE Transactions on Nanotechnology**	Vol. 11, No. 4	Jul. 2012	818 - 829
Chp.	**B**	**4**	**4**	J. Han et al.	Majority Logic: Nanotechnology-Based	Dekker Encyclopedia of Nanoscience and Nanotechnology (Second Edition)	CRC Press	Jun. 2012	2289 - 2298
PhD	**D**	**1**	**0**	L.R. Hook IV	Theory, Design, and Simulation of LINA: A Path Forward for QCA-type Nanoelectronics (UMI 3504406)	University of Oklahoma	Norman, OK, USA	May 2012	1 - 145
Journal	**A**	**8**	**8**	M.M.U. Khan et al.	FastTrack: Towards Nanoscale Fault Masking with High Performance	**IEEE Transactions on Nanotechnology**	Vol. 11, No. 4	Jul. 2012	720 - 730
PhD	**D**	**1**	**0**	S.M.A. Naqvi	Reliable and Fault Tolerant Analog and Mixed Signal Circuit Design (UMI 3507651)	University of Texas at Dallas	Dallas, TX, USA	May 2012	1 - 114
Chp. 18	**A**	**8**	**8**	M. Stanisavljević et al.	Reliability of Nanoelectrinic VLSI	In K. Iniewski (ed.): Advanced Circuits for Emerging Technologies	John Wiley	May 2012	463 - 482
PhD	**D**	**1**	**0**	N. Aymerich	Variability-aware Architectures based on Hardware Redundancy for Nanoscale Reliable Computation	Universidad Politecnica de Catalunya	Barcelona, Spain	Dec. 2013	1 - 149
ieee	**D**	**1**	**0**	T.T. Boon	Probabilistic Neural Computing with Nanoscale CMOS	IEEE Circuits and System Society Malaysia Hi-Tea	Malaysia	29 Jun. 2013	1 - 15
ieee	**D**	**1**	**0**	S. Brkic et al.	Taylor-Kuznetsov Fault-tolerant Memories: A Survey and Results under Correlated Gate Failures	International Conference onTelecommunication in Modern Satellite, Cable and Broadcasting Services	Nis, Serbia	Oct. 2013	455 - 462
PhD	**D**	**1**	**0**	O. Dajani	Emerging Design Methodology and Its Implementation through RNS and QCA	Wayne State University	Detroit, MI, USA	Jan. 2013	1 - 167
ieee	**D**	**1**	**0**	G.R. Voicu and S.D. Cotofana	Towards Heterogenous 3D-Stacked Reliable Computing with von Neumann Multiplexing	IEEE/ACM International Symposium on Nanoscale Architectures	Brooklyn, NY, USA	Jul. 2013	122 - 127
Journal	**A**	**8**	**8**	N. Aymerich and A. Rubio	Reliability and Performance Tunable Architecture: The Partially-Asynchronous RMR (pA-RMR)	**IEEE Transactions on Nanotechnology**	Vol. 13, No. 3	May 2014	617 - 622
Journal	**B**	**4**	**4**	X. Chen et al.	Accurate Reliability Evaluation using Quantum-dot Cellular Automata Probabilistic Transfer Matrix	**Micro & Nano Letters**	Vol. 9, No. 2	Feb. 2014	77 - 82
Journal	**A**	**8**	**8**	J. Han et al.	A Stochastic Computational Approach for Accurate and Efficient Reliability Evaluation	**IEEE Transactions on Computers**	Vol. 63, No. 6	Jun. 2014	1336 - 1350

	PhD	**D**	**1**	**0**	H.K. Kakarla	Fault Free Error Coding Technique for Memory Applications	Koneru Lakshmaiah Education Foundation	Vaddeswaram, Andhra Pradesh, India	Mar. 2014	http://shodhganga.inflibnet.ac.in/handle/10603/25119
	Journal	**A**	**8**	**8**	H. Fujisaka et al.	A Sigma-Delta Domain Lowpass Wave Filter	**IEEE Transactions on Circuits and Systems I: Regular Papers**	Vol. 62, No. 1	Jan. 2015	167 - 176
	Journal	**D**	**1**	**0**	D. Jose et al.	Reliability Improvement of Partitioned VLSI Systems for Fault Tolerance	**International Journal of Applied Engineering Research**	Vol. 10, No. 7	Jul. 2015	18151 - 18165
	arXiv	**D**	**1**	**0**	B. Cruikshank & K. Jacobs	High-Threshold Low-Overhead Fault-Tolerant Classical Computation and the Replacement of Measurements with Unitary Quantum Gates	arXiv:1608.08228v1 [quant-ph]		29 Aug. 2016	1 - 5
	Journal	**A**	**8**	**8**	W. Ibrahim	Identifying the Worst Reliability Input Vectors and the Associated Critical Logic Gates	**IEEE Transactions on Computers**	Vol. 65, No. 6	Jul. 2016	1748 - 1760
338.00			**338**	**264**	**264.00**					

J016	**Journal**				**M.H. Sulieman, and V. Beiu**	**On Single Electron Technology Full Adders**	**IEEE Transactions on Nanotechnology**	**vol. 4, no. 6**	**Nov. 2005**	**669 - 680**
	ieee	**D**	**1**	**0**	Y. Mao and C. Chen	Performance Evaluation and Optimization of Full Adders with Single-Electron Technology	IEEE Canadian Conference on Electrical and Computer Engineering	Ottawa, Canada	7-10 May 2006	2136 - 2139
	ieee	**D**	**1**	**0**	E.R. Taylor et al.	An Investigation into the Maximum Tolerable Error Rate of Majority Gates for Reliable Computation	ACM/IEEE International Conference on Nano Architectures	Boston, MA, USA	17 Jun. 2006	1 - 8
	Journal	**A**	**8**	**8**	J. Hoekstra	On Circuit Theories for Single-Electron Tunneling Devices	**IEEE Transactions on Circuits and Systems I**	Vol. 54, Nov. 11	Nov. 2007	2353 - 2359
	Journal	**D**	**1**	**0**	D. Samanta et al.	Design and Implementation of a Sequence Generator using Single Electron Device based Threshold Logic Gates	**Far East Journal of Electronics and Communications**	Vol. 1, No. 3	Dec. 2007	247 - 258
	acm	**D**	**1**	**0**	M.H. Sulieman	Reliability of single-electron logic gates	ACM Conference on Microelectronics, Nanoelectronics, Optoelectronics	Istanbul, Turkey	27-29 May 2007	50 - 53
	ieee	**D**	**1**	**0**	W.-C. Zhang and N.-J. Wu	Performing Fast Addition and Multiplication by Transferring Single Electrons	IEEE International Conference on Nanotechnology	Hong Kong, China	2-5 Aug. 2007	690 - 694
	PhD	**D**	**1**	**0**	A. Venkataratnam	Design and Simulation of Logic Circuits Using Single Electron Transistors (UMI 3320263)	Michigan Technological University	Houghton, MI, USA	2008	1 - 193
	Journal	**B**	**4**	**4**	C. Choi et al.	Comparative Study on the Energy Efficiency of Logic Gates Based on Single-electron Transistor Technology	**Semiconductor Science and Technology**	Vol. 24, No. 6	Jun. 2009	065007 (1 - 11)
	ieee	**D**	**1**	**0**	G. Deng et al.	Full Adder Design Using Hybrid CMOS-SET Parallel Architectures	IEEE Conference on Nanotechnology	Genoa, Italy	26-30 Jul. 2009	206 - 209
	Journal	**C**	**2**	**0**	W. Zhang and N.-J. Wu	Compact Non-binary Fast Adders Using Single-electron Devices	**Microelectronics Journal**	Vol. 40, No. 8	Aug. 2009	1244 - 1254
	Journal	**B**	**4**	**4**	Y. Chi et al.	Advances in the Modeling of Single Electron Transistors for the Design of Integrated Circuit	**Journal of Nanoscience and Nanotechnology**	Vol. 10, No. 9	Sept. 2010	6131 - 6135
	ieee	**D**	**1**	**0**	G. Deng and C. Chen	Towards Robust Design of Hybrid CMOS-SETs Using Feedback Architectures	IEEE International Conference on Nanotechnology	Seoul, Korea	17-20 Aug. 2010	1125 - 1129
	Journal	**B**	**4**	**4**	G. Deng and C. Chen	Hybrid CMOS-SET Arithmetic Circuit Design Using Coulomb Blockade Oscillation Characteristic	**Journal of Computational and Theoretical Nanoscience**	Vol. 8, no. 8	Aug. 2010	1520 - 1526
	ieee	**D**	**1**	**0**	I.I. Basith et al.	Performance Enhancement of Single Electron Junction 1-bit Full Adder	IEEE International Conference on Electronics, Circuits and Systems	Beirut, Lebanon	11-14 Dec. 2011	157 - 160
	PhD	**D**	**1**	**0**	G. Deng	Hybrid MOS and Single-Electron Transistor Architectures towards Arithmetic Applications	University of Windsor	Windsor, ON, Canada	2011	1 - 140
	Journal	**A**	**8**	**8**	J. Han et al.	On the Reliability of Computational Structures using Majority Logic	**IEEE Transactions on Nanotechnology**	Vol. 10, No. 5	Sep. 2011	1099 - 1112

	Journal	**A**	**8**	**8**		J. Lee et al.	Comparative Study on Energy-Efficiencies of Single-Electron Transistor-Based Binary Full Adders Including Non-Ideal Effects	**IEEE Transactions on Nanotechnology**	Vol. 10, No. 5	May 2011	1180 - 1190
	Journal	**C**	**2**	**0**		M.H. Moaiyeri et al.	Design and analysis of a high-performance CNFET-based Full Adder	**International Journal of Electronics**	Vol. 99, No. 1	Dec. 2011	113 - 130
	Journal	**C**	**2**	**0**		M.J. Sharifi	A Theoretical Study of the Performance of a Single-Electron Transistor Buffer	**IEICE Transactions on Electronics**	Vol. E94-C, No. 6	Jun. 2011	1105 - 1111
	Journal	**C**	**2**	**0**		M.M. Abutaleb	Design and Simulation of Novel TLG-SET Based Configurable Logic Cells	**Microelectronics Journal**	Vol. 43, No. 8	Aug. 2012	537 - 545
	ieee	**D**	**1**	**0**		D. Griveau et al.	Single Electron CMOS-like One Bit Full Adder	IEEE International Conference on Ultimate Integration on Silicon	Grenoble, France	6-7 Mar. 2012	77 - 80
	Journal	**C**	**2**	**0**		M.H. Moaiyeri et al.	Design and Analysis of a High-Performance CNFET-based Full Adder	**International Journal of Electronics**	Vol. 99, No. 1	Jan. 2012	113 - 130
	ebscohost	**D**	**1**	**0**		A. Paulthurai and B. Dharmaraj	Low-Power and High-Performance 1-Bit Set Full-Adder	**Microelectronics and Solid State Electronics**	Vol. 1, No. 4	2012	94 - 97
	Journal	**D**	**1**	**0**		D. Bahrepour and M.J. Sharifi	A Novel High Speed Full Adder Based on Linear Threshold Gate and its Application to a 4-2 Compressor	**Arabian Journal for Science and Engineering**	Vol. 38, No. 11	Nov. 2013	3041 - 3050
	Journal	**B**	**4**	**4**		D. Bahrepour and M.J. Sharifi	High Speed Full Adder Based on Modified Linear Threshold Gate and Its Application to a 4-2 Compressor	**Journal of Computational and Theoretical Nanoscience**	Vol. 10, No. 11	Nov. 2013	2527 - 2535
	Journal	**C**	**2**	**0**		G. Gerousis and A. Grepiotis	Reconfigurable Gate Array Architecture for Logic Functions in Tunneling Transistor Technology	**Microelectronics Journal**	Vol. 44, No. 8	Aug. 2013	706 - 711
	Journal	**C**	**2**	**0**		M. Maleknejad et al.	New CNTFET-Based Arithmetic Cells with Weighted Inputs for High Performance Energy Efficient Applications	**IEICE Transactions on Electronics**	Vol. E96-C, No. 7	Jul. 2013	1019 - 1027
	Journal	**C**	**2**	**0**		Y.S. Mehrabani et al.	A high-speed and high-performance full adder cell based on 32-nm CNFET technology for low voltages	**International Journal of High Performance Systems Architecture**	Vol. 4, No. 4	Jul. 2013	196 - 203
	arXiv	**D**	**1**	**0**		M. Masoudi et al.	Designing High-Speed, Low-Power Full Adder Cells Based on Carbon Nanotube Technology	**International Journal of VLSI Design & Communication Systems**	Vol. 5, No. 5	Oct. 2014	31 - 43
	Journal	**A**	**8**	**8**		K.V. Karthikeyan et al.	Performance Analysis of an Efficient MAC Unit Using CNTFET Technology	**Materials Today**	Vol. 3, No. 6	2016	2525 - 2531
78.00			**78**	**48**	**48.00**						

J017	**Journal**					**V. Beiu, S. Aunet, J. Nyathi, R.R. Rydberg III, and W. Ibrahim**	**Serial Addition: Locally Connected Architectures**	**IEEE Transactions on Circuits & Systems I: Special Issue on Circuits and Computing Architectures for Nanotechnology**	**vol. 54, no. 11**	**Nov. 2007**	**2564 - 2579**
	Journal	**A**	**8**	**8**		R. Cavin et al.	Emerging Research Architectures	**IEEE Computer**	Vol. 41, No. 5	May 2008	33 - 37
	ieee	**D**	**1**	**0**		M.R. Meher et al.	High-speed and Low-power Serial Accumulator for Serial/Parallel Multiplier	IEEE Asia Pacific Conference on Circuits and Systems	Macao, China	30 Nov. - 3 Dec. 2008	176 - 179
	ieee	**D**	**1**	**0**		S. Aunet	Subthreshold Minority-3 Gates and Inverters Used for 32-bit Serial and Parallel Adders Implemented in 90 nm CMOS	IEEE Norchip International Conference	Trondheim, Norway	16-17 Nov. 2009	5397845 (1 - 6)
	ieee	**D**	**1**	**0**		H.K.O. Berge and S. Aunet	Benefits of Decomposing Wide CMOS Transistors into Minimum-size Gates	IEEE Norchip International Conference	Trondheim, Norway	16-17 Nov. 2009	5397795 (1 - 4)

	PhD	**D**	**1**	**0**	M. Stanisavljević	On the Dependability of Nanoscale Circuits and Systems: Methodologies and Circuit Architectures	Ecole Polytechnique Federale de Lausanne	Lausanne, Switzerland	27 Mar. 2009	1 - 238
	Journal	**A**	**8**	**8**	M. Stanisavljević et al.	Optimization of the Averaging Reliability Technique Using Low Redundancy Factors for Nanoscale Technologies	**IEEE Transactions on Nanotechnology**	Vol. 8, No. 3	May 2009	379 - 390
	Journal	**A**	**8**	**8**	H.R. Mahdiani et al.	Bio-Inspired Imprecise Computational Blocks for Efficient VLSI Implementation of Soft-Computing Applications	**IEEE Transactions on Circuits and Systems I**	Vol. 57, No. 4	Apr. 2010	850 - 862
	ieee	**D**	**1**	**0**	S. Aunet	On the Reliability of Ultra Low Voltage Circuits Built from Minority-3 Gates	IEEE European Conference on Circuit Theory and Design	Linköping, Sweden	29-31 Aug. 2011	540 - 543
	ieee	**D**	**1**	**0**	H.K.O. Berge et al.	Muller C-elements Based on Minority-3 Functions for Ultra Low Voltage Supplies	IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems	Cottbus, Germany	13-15 Apr. 2011	195 - 200
	Journal	**A**	**8**	**8**	J. Han et al.	On the Reliability of Computational Structures using Majority Logic	**IEEE Transactions on Nanotechnology**	Vol. 10, No. 5	Sep. 2011	1099 - 1112
	Book	**B**	**4**	**4**	M. Stanisavljević et al.	Reliability of Nanoscale Circuits and Systems: Methodologies and Circuit Architectures	Springer	New York	2011	1 - 195
	US 8,570,061	**D**	**1**	**0**	K. Golke	(N-1)-out-of-N Voter Mux with Enhanced Drive	Honeywell International	Washington, DC, USA	Oct. 2013	1 - 17
	Journal	**A**	**8**	**8**	J. Liang et al.	New Metrics for the Reliability of Approximate and Probabilistic Adders	**IEEE Transactions on Computers**	Vol. 62, No. 9	Sept. 2013	1760 - 1771
17.00			**51**	**44**	**14.67**					

J018	**Journal**				**W. Ibrahim, V. Beiu, and M.H. Sulieman**	**On the Reliability of Majority Gates Full Adders**	**IEEE Transactions on Nanotechnology**	**vol. 7, no. 1**	**Jan. 2008**	**56 - 67**
	Journal	**B**	**4**	**4**	T.J. Dysart and P.M. Kogge	Analyzing the Inherent Reliability of Moderately Sized Magnetic and Electrostatic QCA Circuits Via Probabilistic Transfer Matrices	**IEEE Transactions on VLSI Systems**	Vol. 17, No. 4	Apr. 2009	507 - 516
	Journal	**C**	**2**	**0**	M. Maeen et al.	On the Design of Low Power 1-bit Full Adder Cell	**IEICE Electronics Express**	Vol. 6, No. 16 P	25 Aug. 2009	1148 - 1154
	Journal	**C**	**2**	**0**	M.H. Moaiyeri et al.	Two New Low-power and High-Performance Full Adders	**Journal of Computers**	Vol. 4, No. 2	Feb. 2009	119 - 126
	CSICC-09	**D**	**1**	**0**	M.H. Moaiyeri et al.	New High-Performance Majority Function Based Full Adders	IEEE International CSI Computer Conference	Teheran, Iran	20-21 Oct. 2009	100 - 104
	Journal	**C**	**2**	**0**	K. Navi et al.	Two New Low-power Full Adders Based on Majority-not Gates	**Microelectronics Journal**	Vol. 40, No. 1	Jan. 2009	126 - 130
	Journal	**A**	**8**	**8**	M. Stanisavljević et al.	Optimization of the Averaging Reliability Technique Using Low Redundancy Factors for Nanoscale Technologies	**IEEE Transactions on Nanotechnology**	Vol. 8, No. 3	May 2009	379 - 390
	ieee	**D**	**1**	**0**	M.H. Sulieman	Threshold-Voltage Variations Effects on the Reliability of Nano-scale CMOS Logic Gates	IEEE Nanotechnology Conference	Genoa, Italy	26-30 Jul. 2009	744 - 747
	springer	**D**	**1**	**0**	M.H. Sulieman	On the Reliability of Interconnected CMOS Gates Considering MOSFET Threshold-Voltage Variations	International Conference on Nano-Networks (Springer LNICST 20)	Luzern, Switzerland	18-20 Oct. 2009	251 - 258
	ieee	**D**	**1**	**0**	S. Aunet and A. Hasanbegovic	Memory Elements Based on Minority-3 Gates and Inverters Implemented in 90 nm CMOS	IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems	Vienna, Austria	14-16 Apr. 2010	267 - 272
	ieee	**D**	**1**	**0**	D. Das and H. Rahaman	Crosstalk Analysis in Carbon Nanotube Interconnects and Its Impact on Gate Oxide Reliability	IEEE Asia Symposium on Quality Electronic Design	Penang, Malaysia	3-4 Aug. 2010	272 - 279

Journal	**A**	**8**	**8**	D. Das and H. Rahaman	Analysis of Crosstalk in Single- and Multi-Wall Carbon Nanotube Interconnects and its Impact on Gate Oxide Reliability	**IEEE Transactions on Nanotechnology**	Vol. 10, No. 6	Nov. 2011	1362 - 1370
Journal	**A**	**8**	**8**	J. Han et al.	On the Reliability of Computational Structures using Majority Logic	**IEEE Transactions on Nanotechnology**	Vol. 10, No. 5	Sep. 2011	1099 - 1112
Journal	**D**	**1**	**0**	H. Huang et al.	The Application of Multi-linear Regression Analysis in the Reliability Study of QCA Comparator	**Research and Progress of Solid State Electronics**	Vol. 31, No. 5	2011	460 - 463
Journal	**A**	**8**	**8**	J. Lee et al.	Comparative Study on Energy-Efficiencies of Single-Electron Transistor-Based Binary Full Adders Including Non-Ideal Effects	**IEEE Transactions on Nanotechnology**	Vol. 10, No. 5	May 2011	1180 - 1190
Journal	**C**	**2**	**0**	K. Navi et al.	High-speed Full Adder Based on Minority Function and Bridge Style for Nanoscale	**Integration the VLSI Journal**	Vol. 44, No. 3	Jun. 2011	155 - 162
Book	**B**	**4**	**4**	M. Stanisavljević et al.	Reliability of Nanoscale Circuits and Systems: Methodologies and Circuit Architectures	Springer	New York	2011	1 - 195
Journal	**C**	**2**	**0**	M.M. Abutaleb	Design and Simulation of Novel TLG-SET Based Configurable Logic Cells	**Microelectronics Journal**	Vol. 43, No. 8	Aug. 2012	537 - 545
ieee	**D**	**1**	**0**	N.S.S. Singh et al.	Sensitivity Analysis of Probability Transfer Matrix (PTM) on Same Functionality Circuit Architectures	IEEE 8th International Colloquium on Signal Processing and its Applications	Malacca, Malaysia	23-25 Mar. 2012	250 - 254
ieee	**D**	**1**	**0**	N.S.S. Singh et al.	Accurate Modeling Method to Evaluate Reliability of Nanoscale Circuits	IEEE International Conference on Electron Devices and Solid State Circuit	Bangkok, Thailand	3-5 Dec. 2012	6482862 (1 - 4)
aip	**D**	**1**	**0**	N.S.S. Singh et al.	Reliability Automation Tool (RAT) for Fault Tolerance Computation	AIP International Conference on Fundamental and Applied Sciences	Kuala Lumpur, Malaysia	12-14 Jun. 2012	37 - 42
Chp. 18	**A**	**8**	**8**	M. Stanisavljević et al.	Reliability of Nanoelectrinic VLSI	In K. Iniewski (ed.): Advanced Circuits for Emerging Technologies	John Wiley	May 2012	463 - 482
Journal	**C**	**2**	**0**	S. Wairya et al.	Performance Analysis of High Speed Hybrid CMOS Full Adder Circuits for Low Voltage VLSI Design	**VLSI Design**	Vol. 2012	Jan. 2012	173079 (1 - 18)
Journal	**C**	**2**	**0**	M.M. Abutaleb	Design and Simulation of Novel TLG-SET Based RAM Cell Designs	**Microelectronics Journal**	Vol. 44, No. 6	Jun. 2013	504 - 510
CiteSeerX	**D**	**1**	**0**	E. Alkaldy and K. Navi	Reliability Study of Single Stage Multi-Input Majority Function for QCA	**International Journal of Computer Applications**	Vol. 83, No. 2	Dec. 2013	19 - 23
Journal	**B**	**4**	**4**	D. Bahrepour and M.J. Sharifi	High Speed Full Adder Based on Modified Linear Threshold Gate and Its Application to a 4-2 Compressor	**Journal of Computational and Theoretical Nanoscience**	Vol. 10, No. 11	Nov. 2013	2527 - 2535
CiteSeerX	**D**	**1**	**0**	M.H. Chamansara et al.	High Performance and Low-Power Full Adder	**International Journal of Emerging Science and Engineering**	Vol. 2, No. 1	Nov. 2013	5 - 8
PhD	**D**	**1**	**0**	O. Dajani	Emerging Design Methodology and Its Implementation through RNS and QCA	Wayne State University	Detroit, MI, USA	Jan. 2013	1 - 167
ProQuest	**D**	**1**	**0**	R. Garg et al.	A New Design of Full Adder based on XNOR-XOR Circuit	**International Journal of Computer Applications**	Vol. 66, No.13	Mar. 2013	7 - 10
Journal	**B**	**4**	**4**	P. Kumar	Direct Implementation of an N-qubit Controlled-unitary Gate in a Single Step	**Quantum Information Processing**	Vol. 12, No. 2	Feb. 2013	1201 - 1223
Journal	**A**	**8**	**8**	M. LaRue et al.	Stray Charge in Quantum-dot Cellular Automata: A Validation of the Intercellular Hartree Approximation	**IEEE Transactions on Nanotechnology**	Vol. 12, No. 2	Mar. 2013	225 - 233
Journal	**B**	**4**	**4**	A Sahafi et al.	Efficient Single-Electron Transistor Inverter-Based Logic Circuits and Memory Elements	**Journal of Computational and Theoretical Nanoscience**	Vol. 10, No. 5	May 2013	1171 - 1178

	ieee	D	1	0		P. Wohl and J.A. Waicukauski	Improving Test Generation by Use of Majority Gates	IEEE VLSI Test Symposium	Berkeley, CA, USA	Apr. - May 2013	6548883 (1 - 6)
	PhD	D	1	0		S. Klingler	Spinwellendynamik in mikrostrukturiertem Yttrium-Eisen-Granat	Technischen Universität Kaiserslautern	Kaiserslautern, Germany	Nov. 2014	1 - 117
	Journal	C	2	0		N.S.S. Singh	Programmed Tool for Quantifying Reliability and Its Application in Designing Circuit Systems	**Journal of Electrical and Computer Engineering**	Vol. 2014	May 2014	410758 (1 - 9)
	elsevier	D	1	0		N.S.S. Singh et al.	Error Threshold for Individual Faulty Gates Using Probabilistic Transfer Matrix (PTM)	**AASRI Procedia**	Vol. 9	2014	138 - 145
	Journal	C	2	0		R. Xiao and C. Chen	Gate-Level Circuit Reliability Analysis: A Survey	**VLSI Design**	Vol. 2014	10 Jul. 2014	529392 (1 - 12)
	PhD	D	1	0		H. Astola	Algebraic and Combinatorial Methods for Error-Correcting Codes with Applications to Fault-Tolerant Logic	Tampere University of Technology	Tampere, Finland	27 Nov. 2015	1 - 152
	Journal	A	8	8		W. Ibrahim et al.	Accurate and Efficient Estimation of Logic Circuits Reliability Bounds	**IEEE Transactions on Computers**	Vol. 64, No. 5	May 2015	1217 - 1229
	arXiv	D	1	0		S. Klinger et al.	Spin-Wave Logic Devices Based on Isotropic Forward Volume Magneto-Static Waves	arXiv:1503.04101v1 [cond-mat.mes-hall]		16 Mar. 2015	1 - 4
	Journal	C	2	0		A. Roohi et al.	Design and Evaluation of an Ultra-Area-Efficient Fault-Tolerant QCA Full Adder	**Microelectronics Journal**	Vol. 46, No. 6	Jun. 2015	531 - 542
	ieee	D	1	0		A.A. Vatanjou et al.	Energy Efficient Sub/Near-threshold Ripple-carry Adder in Standard 65 nm CMOS	IEEE Asia Symposium on Quality Electronic Design (ASQED)	Kuala Lumpur	4-5 Aug. 2015	7 - 12
	Journal	B	4	4		Y. Zhang et al.	Modular Design of QCA Carry Flow Adders and Multiplier with Reduced Wire Crossing and Number of Logic Gates	**International Journal of Circuit Theory and Applications**	Vol. 44, No. 7	Jul. 2016	1351 - 1366
119.00			**119**	**80**	**80.00**						

J019	**Journal**					**W. Ibrahim, and V. Beiu**	**Threshold Voltage Variations Make Full Adders Reliabilities Similar**	**IEEE Transactions on Nanotechnology**	**vol. 9, no. 6**	**Nov. 2010**	**664 - 667**
	CiteSeerX	D	1	0		M.H. Chamansara et al.	High Performance and Low-Power Full Adder	**International Journal of Emerging Science and Engineering**	Vol. 2, No. 1	Nov. 2013	5 - 8
	Journal	C	2	0		M Bahadori et al.	A Comparative Study on Performance and Reliability of 32-bit Binary Adders	**Integration, the VLSI Journal**	Vol. 53	Mar. 2016	54 - 67
3.00			**3**	**0**	**0.00**						

J020	**Journal**					**V. Beiu, B.A.M. Madappuram, P.M. Kelly, and L.J. McDaid**	**On Two-layer Brain-inspired Hierarchical Topologies — A Rent's Rule Approach**	**Transactions on High-Performance Embedded Architecture and Compilers (HiPEAC) IV**	**Springer LNCS 6769**	**Jan. 2011**	**311 - 333**
	Journal	B	4	4		J. Partzsch and R. Schuffny	Developing Structural Constraints on Connectivity for Biological Embedded Neural Networks	**Biological Cybernetics**	Vol. 106, No. 3	Mar. 2012	191 - 200
	springer	D	1	0		Y. Katayama et al.	An Energy-Efficient Computing Approach by Filling the Connectome Gap	International Conference on Unconventional Computation and Natural Computation (LNCS 8553)	London, ON, Canada	14-18 Jul. 2014	229 - 241
	arXiv	D	1	0		M. Kyriazis	Technological Integration and Hyper-connectivity: Tools for Promoting Extreme Human Lifespans	arXiv.org > q-bio > arXiv:1402.6910	arXiv	Feb. 2014	1 - 10
	acm	D	1	0		T. Nilsson	Spatial Multiplexing: Solving Information Bottlenecks in Real Neural Systems and the Origin of Brain Rhythms	**International Journal of Adaptive, Resilient and Automatic Systems**	Vol. 5, No. 4	Oct. 2014	46 - 70
	ICONIP-14	A	8	8		G. Tanaka et al.	Hopfield-Type Associative Memory with Sparse Modular Networks	International Conference on Neural Information Processing (LNCS 8834)	Kuching, Malaysia	3-6 Nov. 2014	255 - 262

	Journal	**A**	**8**	**8**		G. Vernizzi et al.	Topological Constraints for E. F. Rent's Work on Microminiature Packaging and Circuitry	**IBM Journal of Research and Development**	Vol. 58, No. 2	Apr. 2014	13 : 1 - 17
11.50			**23**	**20**	**10.00**						

J021	**Journal**					**V. Beiu, and W. Ibrahim**	**Devices and Input Vectors Are Shaping von Neumann Multiplexing**	**IEEE Transactions on Nanotechnology**	**vol. 10, no. 3**	**May 2011**	**606 - 616**
	ProQuest	**D**	**1**	**0**		A. Beg et al.	Effect of Channel Lengthening and Threshold Voltage Variation on a Nanometric Gate's Delay and Power	WorldComp'12 / CDES-12	Las Vegas, NV, USA	16-19 Jul. 2012	55 - 62
	CiteSeerX	**D**	**1**	**0**		M.H. Chamansara et al.	High Performance and Low-Power Full Adder	**International Journal of Emerging Science and Engineering**	Vol. 2, No. 1	Nov. 2013	5 - 8
	ieee	**D**	**1**	**0**		G.R. Voicu and S.D. Cotofana	Towards Heterogenous 3D-Stacked Reliable Computing with von Neumann Multiplexing	IEEE/ACM International Symposium on Nanoscale Architectures	Brooklyn, NY, USA	Jul. 2013	122 - 127
	Journal	**B**	**4**	**4**		A. Arab and Q. Feng	Reliability Research on Micro- and Nano-electromechanical Systems: A Review	**The International Journal of Advanced Manufacturing Technology**	Vol. 74, No. 9-12	Oct. 2014	1679 - 1690
	europment	**D**	**1**	**0**		A. Beg and A. Beg	Investigating the Reliability of Nano-Scaled BDD-Based Gates	International Conference on Circuits, Systems, Signal Processing, Communications and Computers (CSCC)	Venice, Italy	Mar. 2014	84 - 89
	SciChina	**D**	**1**	**0**		J. Xiao et al.	Transistor-level oriented calculation of reliability for generalized gates based on PTM	**Scientia Sinica Informationis**	Vol. 44, No. 10	Oct. 2014	1226 - 1238
	Journal	**A**	**8**	**8**		W. Ibrahim et al.	Accurate and Efficient Estimation of Logic Circuits Reliability Bounds	**IEEE Transactions on Computers**	Vol. 64, No. 5	May 2015	1217 - 1229
	Journal	**A**	**8**	**8**		W. Ibrahim	Identifying the Worst Reliability Input Vectors and the Associated Critical Logic Gates	**IEEE Transactions on Computers**	Vol. 65, No. 6	Jul. 2016	1748 - 1760
25.00			**25**	**20**	**20.00**						

J022	**Journal**					**W. Ibrahim, and V. Beiu**	**Using Bayesian Networks to Accurately Calculate the Reliability of CMOS Gates**	**IEEE Transactions on Reliability**	**vol. 60, no. 3**	**Sept. 2011**	**538 - 549**
	ieee	**D**	**1**	**0**		H. Chen et al.	A Transistor-Level Stochastic Approach for Evaluating the Reliabiltiy of Digital Nanometric CMOS Circuits	IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems	Vancouver, Canada	3-5 Oct. 2011	60 - 67
	ieee	**D**	**1**	**0**		M.H. Sulieman and W. Ibrahim	Design of Low-Power and Reliable Nano Adders	IEEE International Conference on Nanotechnology	Portland, OR, USA	15-18 Aug. 2011	441 - 444
	ieee	**D**	**1**	**0**		J. Liang et al.	Design and Reliability Analysis of Multiple Valued Logic Gates using Carbon Nanotube FETs	IEEE/ACM International Symposium on Nanoscale Architectures	Amsterdam, The Netherlands	4-6 Jul. 2012	131 - 138
	Journal	**B**	**4**	**4**		L. Meng et al.	A Multi-agent Based Approach to Reliability Prediction of Train's Control and Monitoring Software System	**International Journal of Digital Content Technology and its Applications**	Vol. 6, No. 12	Jul. 2012	149 - 157
	CiteSeerX	**D**	**1**	**0**		M.H. Chamansara et al.	High Performance and Low-Power Full Adder	**International Journal of Emerging Science and Engineering**	Vol. 2, No. 1	Nov. 2013	5 - 8
	acm	**D**	**1**	**0**		W. Ibrahim	Accurate and Effective Algorithm for Estimating the Reliability of Digital Combinational Circuits	ACM Annual Simulation Symposium (Spring Simulation Multi-Conference SpringSim'13)	San Diego, CA, USA	Apr. 2013	65 - 72
	Journal	**B**	**4**	**4**		A. Arab and Q. Feng	Reliability Research on Micro- and Nano-electromechanical Systems: A Review	**The International Journal of Advanced Manufacturing Technology**	Vol. 74, No. 9-12	Oct. 2014	1679 - 1690
		D	**1**	**0**		R. Di et al.	Discrete Bayesian network parameter learning based on monotonic constraint	**Systems Engineering and Electronics**	Vol. 36, No. 2	Feb. 2014	272 - 277
	Journal	**B**	**4**	**4**		Z.-G. Guo et al.	Learning Bayesian Network Parameters under Dual Constraints from Small Data Set	**Acta Automatica Sinica**	Vol. 40, No. 7	Jul. 2014	1509 - 1516

	ieee	D	1	0		N. Cucu-Laurenciu and S.D. Cotofana	Probability Density Function Based Reliability Evaluation of Large-Scale Ics	IEEE/ACM International Symposium on Nanoscale Architectures (NanoArch)	Paris, France	Jul. 2014	157 - 162
	SciChina	D	1	0		J. Xiao et al.	Transistor-level oriented calculation of reliability for generalized gates based on PTM	**Scientia Sinica Informationis**	Vol. 44, No. 10	Oct. 2014	1226 - 1238
	Journal	A	8	8		W. Ibrahim et al.	Accurate and Efficient Estimation of Logic Circuits Reliability Bounds	**IEEE Transactions on Computers**	Vol. 64, No. 5	May 2015	1217 - 1229
	Journal	B	4	4		Y. Yang et al.	Learning BN Parameters with Small Data Sets Based by Data Reutilization	**Acta Automatica Sinica**	Vol. 41, No. 12	Dec. 2015	2058 - 2071
	Chp.	B	4	4		Z. Guo et al.	Learning Bayesian Network Parameters from Small Data Set: A Spatially Maximum a Posteriori Method	Advanced Methodologies for Bayesian Networks	Springer LNCS 9505	Jan. 2016	32 - 45
	Journal	C	2	0		Z. Guo et al.	Learning Bayesian Network Parameters from Small Data Set: An Adaptive Method	**Control Theory & Applications**	Vol. 33, No. 7	Jul. 2016	945 - 955
38.00			**38**	**28**	**28.00**						

J023	**Journal**					**W. Ibrahim, V. Beiu, and A. Beg**	**GREDA: A Fast and More Accurate CMOS Gates Reliability EDA Tool**	**IEEE Transactions on Computer-Aided Design of Integrated Circuits & Systems**	**vol. 31, no. 4**	**Apr. 2012**	**509 - 521**
	ieee	D	1	0		J. Liang et al.	Design and Reliability Analysis of Multiple Valued Logic Gates using Carbon Nanotube FETs	IEEE/ACM International Symposium on Nanoscale Architectures	Amsterdam, The Netherlands	4-6 Jul. 2012	131 - 138
	Journal	C	2	0		M. Alawad et al.	Stochastically Estimating Modular Criticality in Large-Scale Logic Circuits using Sparsity Regularization and Compressive Sensing	**Journal of Low Power Electronics and Applications**	Vol. 5, No. 1	Mar. 2015	3 - 37
	europment	D	1	0		A. Beg and A. Beg	Investigating the Reliability of Nano-Scaled BDD-Based Gates	International Conference on Circuits, Systems, Signal Processing, Communications and Computers (CSCC)	Venice, Italy	Mar. 2014	84 - 89
	ProQuest	D	1	0		A. Beg and A. Beg	Reliability of Nano-Scaled Logic Gates Based on Binary Decision Diagrams	International Conference on Modeling, Simulation and Visualization Methods (MSV), part of WORLDCOMP'14	Las Vegas, NV, USA	Jul. 2014	1 - 7
	ieee	D	1	0		C. Dezan and S. Zermani	Stochastic Reliability Evaluation of Sea-of-Tiles Based on Double Gate Controllable-Polarity FETs	IEEE/ACM International Symposium on Nanoscale Architectures (NanoArch)	Paris, France	Jul. 2014	169 - 170
	Journal	C	2	0		J. Xiao et al.	A Defect Analysis-Oriented Relation Model of Circuit Yield and Reliability	**Acta Electronica Sinica (Chinese Journal of Electronics)**	Vol. 42, No. 4	2014	747 - 755
	SciChina	D	1	0		J. Xiao et al.	Transistor-level oriented calculation of reliability for generalized gates based on PTM	**Scientia Sinica Informationis**	Vol. 44, No. 10	Oct. 2014	1226 - 1238
	ProQuest	D	1	0		Y. Bai et al.	Optimally Fortifying Logic Reliability through Criticality Ranking	**Electronics**	Vol. 4, No. 1	Jan. 2015	150 - 172
	Journal	A	8	8		W. Ibrahim et al.	Accurate and Efficient Estimation of Logic Circuits Reliability Bounds	**IEEE Transactions on Computers**	Vol. 64, No. 5	May 2015	1217 - 1229
18.00			**18**	**8**	**8.00**						

J024	**Journal**					**W. Ibrahim, V. Beiu, and A. Beg**	**Optimum Reliability Sizing for CMOS Gates**	**IEEE Transactions on Reliability**	**vol. 61, no. 3**	**Sept. 2012**	**675 - 686**
	CSCWD-13	B	4	4		A. Beg et al.	A Collaborative Platform for Facilitating Standard Cell Characterization	IEEE International Conference on Computer Supported Cooperative Work in Design	Whistler, BC, Canada	Jun. 2013	202 - 206
	europment	D	1	0		A. Beg and A. Beg	Investigating the Reliability of Nano-Scaled BDD-Based Gates	International Conference on Circuits, Systems, Signal Processing, Communications and Computers (CSCC)	Venice, Italy	Mar. 2014	84 - 89
	ProQuest	D	1	0		A. Beg and A. Beg	Reliability of Nano-Scaled Logic Gates Based on Binary Decision Diagrams	International Conference on Modeling, Simulation and Visualization Methods (MSV), part of WORLDCOMP'14	Las Vegas, NV, USA	Jul. 2014	1 - 7

6.00			**6**	**4**	**4.00**						
J025	**Journal**					**G. Wendin, D. Vuillaume, M. Calame, S. Yitzchaik, C. Gamrat, G. Cuniberti, and V. Beiu**	**SYMONE Project: SYnaptic MOlecular NEtworks for Bio-inspired Information Processing**	**Journal of Unconventional Computing**	**vol. 8, no. 4**	**Nov. 2012**	**325 - 332**
	arXiv	**D**	**1**	**0**		Z. Konkoli and G. Wendin	Toward Bio-inspired Information Processing with Networks of Nano-scale Switching Elements	arXiv:1311.6259v1 [cs.ET]		Nov. 2013	1 - 34
	aip	**D**	**1**	**0**		V. Erokhin	Organic Memristive Device as Key Element for Neuromorphic Networks	International Conference on Numerical Analysis and Applied Mathematics (ICNAAM)	Rhodes, Greece	22-28 Sept. 2014	280006 (1 - 4)
	e-mrs	**D**	**1**	**0**		Z. Konkoli and G. Wendin	Bio-inspired information processing with memristor switching networks	European Materials Research Society Spring Meeting (E-MRS)	Lille, France	May 2014	http://www.european-mrs.com/meetings/archives/2014/2014-spring
	Journal	**C**	**2**	**0**		Z. Konkoli and G. Wendin	On Information Processing with Networks of Nano-Scale Switching Elements	**International Journal of Unconventional Computing**	Vol. 10, No. 5-6	Jun. 2014	405 - 428
	Book	**B**	**4**	**4**		A. Adamatzky	Atlas of Physarum Computing	World Scientific ISBN: 978-981-4675-31-4	Singapore	May 2015	1 - 128
	Journal	**A**	**8**	**8**		Y. Viero et al.	High Conductance Ratio in Molecular Optical Switching of Functionalized Nanoparticle Self-Assembled Nanodevices	**The Journal of Physical Chemistry C**	Vol. 119, No. 36	Aug. 2015	21173 - 21183
	Chp.	**B**	**4**	**4**		M. Dale et al.	Reservoir Computing as a Model for In-Materio Computing	In "Advances in Unconventional Computing"	Springer	Jul. 2016	533 - 571
4.20			**21**	**16**	**3.20**						
J026	**Journal**					**M. Tache, V. Beiu, W. Ibrahim, F. Kharbash, and M. Alioto**	**Enhancing the Static Noise Margins by Sizing Length for Ultra-Low Voltage/Power/Energy Gates**	**Journal of Low Power Electronics**	**vol. 10, no. 1**	**Mar. 2014**	**137 - 148**
	ieee	**D**	**1**	**0**		A.A. Vatanjou et al.	Energy Efficient Sub/Near-threshold Ripple-carry Adder in Standard 65 nm CMOS	IEEE Asia Symposium on Quality Electronic Design (ASQED)	Kuala Lumpur	4-5 Aug. 2015	7 - 12
0.33			**1**	**0**	**0.00**						
J027	**Journal**					**L. Dauş, and V. Beiu**	**Lower and Upper Reliability Bounds for Consecutive-k-out-of-n:F Systems**	**IEEE Transactions on Reliability**	**vol. 64, no. 3**	**Sept. 2015**	**1128 - 1135**
	arXiv	**D**	**1**	**0**		S. Cowell	A Formula for the Reliability of a d-dimensional Consecutive-k-out-of-n:F System	**International Journal of Combinatorics**	Vol. 2015	2015	art. 140909 (pp. 1 - 5)
1.00			**1**	**0**	**0.00**						
0017	**INFO-IASI-89**					**V. Beiu**	**From Systolic Arrays to Neural Networks**	**International Symposium on Informatics**	**Iaşi, Romania**	**19-21 Oct. 1989**	
	Journal	**C**	**2**	**0**		T.S. Balaban et al.	Computer generation of acyclic graphs based on local vertex invariants and topological indices	**Journal of Mathematical Chemistry**	Vol. 11, No. 1	1992	79 - 105
2.00			**2**	**0**	**0.00**						

0024	**CIMCA-99**					**V. Beiu, J. Frigo, and K.R. Moore**	**On the Reliability of Nervous Nets**	**International Conference on Computational Intelligence for Modeling Control and Automation**	**Vienna, Austria**	**17-19 Feb. 1999**	
	aiaa	**D**	**1**	**0**		M.L. Rilee et al.	Evolving a Self-Organizing Neuromechanical System for Self-Healing Aerospace Structures	Conference on Micro-Nano-Technologies	Monterey, USA	1-5 Nov. 2004	1 - 8
	arXiv	**D**	**1**	**0**		E.A. Rietman and R.W. Hillis	Neural Computation with Rings of Quasiperiodic Oscillators	Physical Sciences Inc. PSI SR-1278	Andover, MA, USA	27 Nov. 2006	1 - 54
	CiteSeerX	**D**	**1**	**0**		M.A. Panait and T. Tudorache	A Simple Neural Network Solar Tracker for Optimizing Conversion Efficiency in Off-Grid Solar Generators	International Conference on Renewable Energies and Power Quality	Valencia, Spain	12-14 Mar. 2008	1 - 5
	ieee	**D**	**1**	**0**		A. Harris and J.M. Conrad	Hybrid Control of a Simple Walking Autonomous Robot	IEEE Southeast Conference	Atlanta, GA, USA	5-8 Mar. 2009	420 - 423
	PhD	**D**	**1**	**0**		B.R. Hemes	Locomotion of Serial Multiply-Actuated Tumbling Robots (UMI 3465110)	University of Minnesota	Minneapolis, MN, USA	Jun. 2011	1 - 243
	Journal	**D**	**1**	**0**		P. Vadakkepat et al.	Analogue Neuronal Network in a Biomorphic Machine: Modelling and Simulation in ADAMs	**Transactions of the Institute of Measurement and Control**	Vol. 34, No. 2-3	Apr.-May 2012	184 - 212
6.00			**6**	**0**	**0.00**						

0031	**NanoArch-05**					**V. Beiu, S. Aunet, R. Rydberg III, A. Djupdal, and J. Nvathi**	**The Vanishing Majority Gate – Trading Power and Speed for Reliability**	**IEEE International Workshop on Design and Test of Defect-Tolerant Nanoscale Architectures NanoArch'05**	**Palm Springs, CA, USA**	**1 May 2005**	
	ifip	**D**	**1**	**0**		S. Aunet and Y. Berg	Three Sub-fJ Power-Delay-Product Subthreshold CMOS Gates	IFIP (International Federation for Information Processing) VLSI-SoC	Perth, Australia	17-19 Oct. 2005	465 - 470
	ieee	**D**	**1**	**0**		E.R. Taylor et al.	An Investigation into the Maximum Tolerable Error Rate of Majority Gates for Reliable Computation	ACM/IEEE International Conference on Nano Architectures	Boston, MA, USA	17 Jun. 2006	1 - 8
	Journal	**A**	**8**	**8**		C. Chen	Reliability-Driven Gate Replication for Nanometer-Scale Digital Logic	**IEEE Transactions on Nanotechnology**	Vol. 6	May 2007	303 - 308
	csl	**D**	**1**	**0**		S. Ghosh and P.D. Lincoln	Low-Density Parity Check Codes for Error Correction in Nanoscale Memory	SRI CS Laboratory Technical Report	Menlo Park, CA, USA	25 Sept. 2007	1 - 22
	PhD	**D**	**1**	**0**		A. Djupdal	Evolving Static Hardware Redundancy for Defect Tolerant FPGAs	Norwegian University of Science and Technology	Trondheim, Norway	25 Apr. 2008	1 - 124
	PhD	**D**	**1**	**0**		M. Stanisavljević	On the Dependability of Nanoscale Circuits and Systems: Methodologies and Circuit Architectures	Ecole Polytechnique Federale de Lausanne	Lausanne, Switzerland	27 Mar. 2009	1 - 238
	Journal	**A**	**8**	**8**		M. Stanisavljević et al.	Optimization of the Averaging Reliability Technique Using Low Redundancy Factors for Nanoscale Technologies	**IEEE Transactions on Nanotechnology**	Vol. 8, No. 3	May 2009	379 - 390
	ieee	**D**	**1**	**0**		M. Stanisavljević et al.	Optimization of Nanoelectronic Systems Reliability Under Massive Defect Density Using Distributed R-fold Modular Redundancy (DRMR)	IEEE International Symposium on defect and Fault Tolerance in VLSI Systems	Chicago, IL, USA	7-9 Oct. 2009	340 - 348
	ieee	**D**	**1**	**0**		S. Ghosh and P.G. Lincoln	Dynamic LDPC Codes for Nanoscale Memory with Varying Fault Arrival Rates	IEEE International Conference on Design & Technology of Integrated Systems in Nanoscale Era	Athens, Greece	6-8 Apr. 2011	1 - 4
	Book	**B**	**4**	**4**		M. Stanisavljević et al.	Reliability of Nanoscale Circuits and Systems: Methodologies and Circuit Architectures	Springer	New York	2011	1 - 195
	ieee	**D**	**1**	**0**		M. Moradi et al.	An Applicable High-Efficient CNTFET-Based Full Adder Cell for Practical Environments	IEEE International Symposium on Computer Architecture and Digital Systems	Shiraz, Fars, Iran	2-3 May 2012	7 - 12

	US 8,570,061	**D**	**1**	**0**		K. Golke	(N-1)-out-of-N Voter Mux with Enhanced Drive	Honeywell International	Washington, DC, USA	Oct. 2013	1 - 17
	CiteSeerX	**D**	**1**	**0**		S.Vaishnavi et al.	Elimination of Silent Data Corruption by Improved Error Detection using Difference Set Codes for Memories	**International Journal of Engineering and Advanced Technology**	Vol. 2, No. 3	Feb. 2013	111 - 114
10.00			**30**	**20**	**6.67**						
O032	**IIT-05**					**V. Beiu, J. Nyathi, and S. Aunet**	**Sub-Pico (Femto) Joule Switching: High-Speed Reliable CMOS Circuits Are Feasible**	**International Conference on Innovations in Information Technology**	**Dubai, UAE**	**26-28 Sept. 2005**	
	ieee	**D**	**1**	**0**		P.K. Sharma and M.S.-W. Chen	A 6b 800MS/s 3.62mW Nyquist AC-coupled VCO-Based ADC in 65nm CMOS	IEEE Custom Integrated Circuits Conference	San Jose, CA, USA	Sept. 2013	1 - 4
	Journal	**C**	**2**	**0**		S.M. Sharroush	Analysis of the Subthreshold CMOS Logic Inverter	**Ain Shams Engineering Journal**	Advanced access	30 Jun. 2016	1 - 17
3.00			**3**	**0**	**0.00**						
O042	**DFR-12**					**V. Beiu, W. Ibrahim, A. Beg, and M. Tache**	**On Sizing Transistors for Threshold Voltage Variations**	**International Workshop on Design for Reliability (DFR'12 in conjunction with HiPEAC'12)**	**Paris, France**	**23-25 Jan. 2012**	
	Journal	**B**	**4**	**4**		A. Beg	Automating the sizing of transistors in CMOS gates for low-power and high-noise margin operation	**International Journal of Circuit Theory and Applications**	Vol. 43, No. 11	Nov. 2015	1637 - 1654
2.00			**4**	**4**	**2.00**						
O044	**ULSIWS-14**					**L. Dauş, and V. Beiu**	**A Survey of Consecutive-k-out-of-n Systems Bounds**	**International Workshop on Post-Binary ULSI Systems ULSIWS'14 (IEEE International Symposium on Multiple-Valued Logic ISMVL'14)**	**Bremen, Germany**	**18-21 May 2014**	
	arXiv	**D**	**1**	**0**		S. Cowell	A Formula for the Reliability of a d-dimensional Consecutive-k-out-of-n:F System	**International Journal of Combinatorics**	Vol. 2015	2015	140909 (1 - 5)
1.00			**1**	**0**	**0.00**						
P002	**US 6,205,458**					**V. Beiu**	**Adder and Multiplier Circuits Employing Logic Gates Having Discrete, Weighted Inputs and Methods of Performing Combinatorial Operations Therewith**	**RN2R**	**Washington, DC, USA**	**20 Mar. 2001**	**1 - 14**
	Journal	**A**	**8**	**8**		S. Draghici	On the Capabilities of Neural Networks Using Limited Precision Weights	**Neural Networks**	Vol. 15, No. 3	Apr. 2002	395 - 414
8.00			**8**	**8**	**8.00**						
P003	**US 6,259,275**					**V. Beiu**	**Logic Gate Having Reduced Power Dissipation and Method of Operation Thereof**	**RN2R**	**Washington, DC, USA**	**10 Jul. 2001**	**1 - 19**
	Journal	**A**	**8**	**8**		S. Draghici	On the Capabilities of Neural Networks Using Limited Precision Weights	**Neural Networks**	Vol. 15, No. 3	Apr. 2002	395 - 414
	WO 2003010642	**D**	**1**	**0**		Z. Ahsanullah et al.	Method and apparatus for controlling signal states and leakage current during a sleep mode	World Intellectual Property Organization (WO 2003010642 A2)	Geneva, Switzerland	6 Feb. 2003	http://www.google.com/patents/WO2003010642A3
	US 6,552,573	**D**	**1**	**0**		J.B. Barton	System and Method for Reducing Leakage Current in Dynamic Circuits with Low Threshold Voltage Transistors	Texas Instruments	Washington, USA	22 Apr. 2003	1 - 9
	US 6,566,906	**D**	**1**	**0**		C.K. Hwang et	Specialized Programmable Logic Region with Low-Power Mode	Altera	Washington,	20 May 2003	1 - 13

	US 6,714,042	**D**	**1**	**0**		C.K. Hwang et al.	Specialized Programmable Logic Region with Low-Power Mode	Altera	Washington, USA	30 Mar. 2004	1 - 11
	US 6,882,200	**D**	**1**	**0**		Z. Ahsanullah et al.	Controlling Signal States and Leakage Current During a Sleep Mode	Intel	Washington, DC, USA	19 Apr. 2005	1 - 11
	US 6,937,062	**D**	**1**	**0**		C.K. Hwang et al.	Specialized Programmable Logic Region with Low-power Mode	Altera Co.	Washington, DC, USA	30 Aug. 2005	1 - 10
	US 7,082,592	**D**	**1**	**0**		K. Tharmalingam	Method for Programming Programmable Logic Device Having Specialized Functional Blocks	US Patent, Altera	Washington, DC, USA	25 Jul. 2006	1 - 14
	US 7,417,481	**D**	**1**	**0**		Z. Ahsanullah et al.	Controlling Signal States and Leakage Current During a Sleep Mode	Intel	Washington, DC, USA	26 Aug. 2008	1 - 11
	US 7,698,358	**D**	**1**	**0**		M. Langhammer et al.	Programmable Logic Device with Specialized Functional Block	Altera Corp.	Washington, DC, USA	13 Apr. 2010	1 - 12
	US 7,977,969	**D**	**1**	**0**		M. Lueger and P. Trattler	Circuit Arrangement and Method for Evaluating a Data Signal	AustriaMicroSystem AG	Washington, DC, USA	12 Jul. 2011	1 - 14
	US 8,614,599	**D**	**1**	**0**		A.M. Bekele et al.	Method and Apparatus for Powering Down a Dual Supply Current Source	Xilinx, Inc.	Washington, DC, USA	Dec. 2013	1 - 9
	US 8,364,738	**D**	**1**	**0**		M. Langhammer et al.	Programmable Logic Device with Specialized Functional Block	Altera	Washington, DC, USA	Jan. 2013	1 - 12
20.00			**20**	**8**	**8.00**						
P007	**US 6,430,585**					**V. Beiu**	**Noise Tolerant Conductance-Based Logic Gate and Methods of Operation and Manufacturing Thereof**	**RN2R**	**Washington, DC, USA**	**6 Aug. 2002**	**1 - 16**
	US 8,068,367	**D**	**1**	**0**		J.R. Baker	Reference Current Sources	Micron Technology, Inc.	Washington, DC, USA	29 Nov. 2011	1 - 30
	US 20120068758	**D**	**1**	**0**		J.R. Baker	Reference Current Sources	Micron Technology, Inc.	Washington, DC, USA	22 Mar. 2012	1 - 29
	US 8,675,413	**D**	**1**	**0**		R.J. Baker	Reference Current Sources	Micron Technology, Inc.	Washington, DC, USA	18 Mar. 2014	1 - 29
	US 8,879,327	**D**	**1**	**0**		R.J. Baker	Reference Current Sources	Micron Technology, Inc.	Washington, DC, USA	4 Nov. 2014	1 - 29
4.00			**4**	**0**	**0.00**						
P009	**US 6,502,120**					**V. Beiu**	**Adder Circuits Employing Logic Gates Having Discrete Weighted Inputs and a Method of Operation Therewith**	**RN2R**	**Washington, DC, USA**	**31 Dec. 2002**	**1 - 13**
	US 7,621,963	**D**	**1**	**0**		B.J. Simon et al.	Composite Bone Graft Material	EBI LLC	Washington, DC, USA	24 Nov. 2009	1 - 23
1.00			**1**	**0**	**0.00**						
P010	**US 6,516,331**					**V. Beiu**	**Microprocessor and a Digital Signal Processor Including Adder and Multiplier Circuits Employing Logic Gates Having Discrete and Weighted Inputs**	**RN2R**	**Washington, DC, USA**	**4 Feb. 2003**	**1 - 14**
	CiteSeerX	**D**	**1**	**0**		H. Thapliyal, H.R. Arabnia	A Time-Area-Power Efficient Multiplier and Square Architecture Based on Ancient Indian Vedic Mathematics	International Conference on Embedded Systems and Applications	Las Vegas, USA	21-24 Jun. 2004	434 - 439
	CiteSeerX	**D**	**1**	**0**		H. Thapliyal and M.B Srinivas	High Speed Efficient NxN Bit Parallel Hierarchical Overlay Multiplier Architecture Based on Ancient Indian Vedic Mathematics	Enformatika (Transactions on Engineering, Computing and Technology)	Vol. 2	Dec. 2004	225 - 228

US 6,901,720	**D**	**1**	**0**	T. Lechner and L. Pauls	Beverage Bottling Plant for Filling Bottles with a Liquid Beverage Filling Material, and Apparatus for Attaching Carrying Grips to Containers with Filled Bottles	US Patent, KHS Maschinen- und Anlagenbau AG	Washington, DC, USA	7 Jun, 2005	1 - 17
ieee	**D**	**1**	**0**	H. Thapliyal et al.	A Low Power Decomposed Hierarchical Multiplier Architecture Embedding Multiplexer Based Full Adders	IEEE Midwest Symposium on Circuits and Systems	Cincinnati, OH, USA	7-10 Aug. 2005	1485 - 1488
US 7,065,938	**D**	**1**	**0**	L. Deckert	Beverage Bottling Plant for Filling Bottles with a Liquid Beverage Filling Material, and a Container Filling Plant Container Information Adding Station, such as, a Labeling Station Having a Gripper Arrangement, Configured to Add Information to Containers, such as, Bottles and Cans	US Patent, KHS Maschinen- und Anlagenbau AG	Washington, DC, USA	27 Jun. 2006	1 - 27
US 7,062,894	**D**	**1**	**0**	H. Loffler	Beverage Bottling Plant for Filling Bottles with a Liquid Beverage Filling Material, and a Container Filling Plant Container Information Adding Station, such as, a Labeling Station Having a Sleeve Label Cutting Arrangement, Configured to Add Information to Containers, such as, Bottles and Cans	US Patent, KHS Maschinen- und Anlagenbau AG	Washington, DC, USA	20 Jun. 2006	1 - 18
US 7,255,141	**D**	**1**	**0**	H. Becker	Beverage Bottling Plant for Filling Bottles with a Liquid Beverage Filling Material, a Container Filling Plant Container Filling Machine, and a Filter Apparatus for Filtering a Liquid Beverage	KHS Maschinen-und Anlagenbau AG	Washington, DC, USA	14 Aug. 2007	1 - 22
DE102007030569	**D**	**1**	**0**	M. Lueger and P. Trattler	Schaltungsanordnung und Verfahren zum Auswerten eines Datensignals	AustriaMicroSystem AG	Germany	8 Jan. 2009	https://google.com/patents/DE102007030569B4
US 7,565,525	**D**	**1**	**0**	M. Vorbach and R. Munch	Runtime Configurable Arithmetic and Logic Cell	Pact XPP Technologies AG	Washington, DC, USA	21 Jul. 2009	1 - 23
US 7,595,659	**D**	**1**	**0**	M. Vorbach et al.	Logic Cell Array and Bus System	Pact XPP Technologies AG	Washington, DC, USA	29 Sept. 2009	1 - 24
US 7,650,448	**D**	**1**	**0**	M. Vorbach and R. Munch	I/O and Memory Bus System for DFPS and Units with Two- or Multi-Dimensional Programmable Cell Architectures	Pact XPP Technologies AG	Washington, DC, USA	19 Jan. 2010	1 - 39
US 7,657,861	**D**	**1**	**0**	M. Vorbach et al.	Method and Device for Processing Data	Pact XPP Technologies AG	Washington, DC, USA	2 Feb. 2010	1 - 46
US 7,657,877	**D**	**1**	**0**	M. Vorbach et al.	Method for Processing Data	Pact XPP Technologies AG	Washington, DC, USA	2 Feb. 2010	1 - 30
US 7,782,087	**D**	**1**	**0**	M. Vorbach	Reconfigurable Sequencer Structure	Pact XPP Technologies AG	Washington, DC, USA	24 Aug. 2010	1 - 24
US 7,822,881	**D**	**1**	**0**	M. Vorbach and R. Münch	Process for Automatic Dynamic Reloading of Data Flow Processors (DFPs) and Units with Two- or Three-dimensional Programmable Cell Architectures (FPGAs, DPGAs, and the like)	Pact XPP Technologies AG	Washington, DC, USA	26 Oct. 2010	1 - 41
US 7,844,796	**D**	**1**	**0**	M. Vorbach and A. Thomas	Data Processing Device and Method	Pact XPP Technologies AG	Washington, DC, USA	30 Nov. 2010	1 - 80
US 7,879,247	**D**	**1**	**0**	H. Becker	Beverage Bottling Plant for Filling Bottles with a Liquid Beverage Filling Material, a Container Filling Plant Container Filling Machine, and a Filter Apparatus for Filtering a Liquid Beverage	KHS Maschinen- und Anlagenbau AG	Washington, DC, USA	1 Feb. 2011	1 - 21
US 7,991,820	**D**	**1**	**0**	L.I. Sohay	One Step Binary Summarizer	L.I. Sohay	Washington, DC, USA	2 Aug. 2011	1 - 31

US 7,899,962	**D**	**1**	**0**	M. Vorbach and R. Münch	I/O and Memory Bus System for DFPs and Units with Two- or Multi-dimensional Programmable Cell Architectures	Pact XPP Technologies AG	Washington, DC, USA	1 Mar. 2011	1 - 52
US 7,928,763	**D**	**1**	**0**	M. Vorbach	Multi-core Processing System	Pact XPP Technologies AG	Washington, DC, USA	19 Apr. 2011	1 - 26
US 8,058,899	**D**	**1**	**0**	M. Vorbach et al.	Logic Cell Array and Bus System	Pact XPP Technologies AG	Washington, DC, USA	15 Nov. 2011	1 - 34
US 8,069,373	**D**	**1**	**0**	M. Vorbach	Method for Debugging Reconfigurable Architectures	Pact XPP Technologies AG	Washington, DC, USA	29 Nov. 2011	1 - 26
US 8,156,312	**D**	**1**	**0**	M. Vorbach and R. Munch	Processor Chip for Reconfigurable Data Processing, for Processing Numeric and Logic Operations and Including Function and Interconnection Control Units	M. Vorbach and R. Munch	Washington, DC, USA	10 Apr. 2012	1 - 40
US 8,127,061	**D**	**1**	**0**	M. Vorbach et al.	Bus Systems and Reconfiguration Methods	M. Vorbach et al.	Washington, DC, USA	28 Feb. 2012	1 - 39
US 8,230,411	**D**	**1**	**0**	M. Vorbach and A. Nuckel	Method for Interleaving a Program Over a Plurality of Cells	M. Vorbach and A. Nuckel	Washington, DC, USA	24 Jul. 2012	1 - 72
US 8,312,200	**D**	**1**	**0**	M. Vorbach and A. Nuckel	Processor Chip Including a Plurality of Cache Elements Connected to a Plurality of Processor Cores	M. Vorbach and A. Nuckel	Washington, DC, USA	13 Nov. 2012	1 - 74
US 8,281,108	**D**	**1**	**0**	M. Vorbach and V. Baumgarte	Reconfigurable General Purpose Processor Having Time Restricted Configurations	M. Vorbach and V. Baumgarte	Washington, DC, USA	2 Oct. 2012	1 - 29
US 8,312,301	**D**	**1**	**0**	M. Vorbach and V. Baumgarte	Methods and Devices for Treating and Processing Data	M. Vorbach and V. Baumgarte	Washington, DC, USA	13 Nov. 2012	1 - 31
US RE44,365	**D**	**1**	**0**	M. Vorbach and R.M. Munch	Method of Self-synchronization of Configurable Elements of a Programmable Module	Pact XPP Technologies AG	Washington, DC, USA	Jul. 2013	1 - 42
US 8,686,549	**D**	**1**	**0**	M. Vorbach	Reconfigurable Elements	Pact XPP Technologies AG	Washington, DC, USA	Apr. 2014	1 - 59
US RE45,109 E	**D**	**1**	**0**	M. Vorbach and R.M. Münch	Method of Self-synchronization of Configurable Elements of a Programmable Module	Pact XPP Technologies AG	Washington, DC, USA	2 Sept. 2014	1 - 35
US 8,869,121	**D**	**1**	**0**	M. Vorbach et al.	Method for the Translation of Programs for Reconfigurable Architectures	Pact XPP Technologies AG	Washington, DC, USA	21 Oct. 2014	1 - 40
US RE45,223	**D**	**1**	**0**	M. Vorbach and R.M. Münch	Method of Self-Synchronization of Configurable Elements of a Programmable Module	Pact XPP Technologies AG	Washington, DC, USA	28 Oct. 2014	1 - 39
US 8,726,250	**D**	**1**	**0**	M. Vorbach and A. Nuckel	Configurable Logic Integrated Circuit Having a Multidimensional Structure of Configurable Elements	Pact XPP Technologies AG	Washington, DC, USA	13 May 2014	1 - 73
US 8,812,820	**D**	**1**	**0**	M. Vorbach and A. Thomas	Data Processing Device and Method	Pact XPP Technologies AG	Washington, DC, USA	19 Aug. 2014	1 - 83
US 8,819,505	**D**	**1**	**0**	M. Vorbach and R.M. Münch	Data Processor Having Disabled Cores	Pact XPP Technologies AG	Washington, DC, USA	26 Aug. 2014	1 - 43
US 8,914,590	**D**	**1**	**0**	M. Vorbach et al.	Data Processing Method and Device	Pact XPP Technologies AG	Washington, DC, USA	16 Dec. 2014	1 - 147
US 9,037,807	**D**	**1**	**0**	M. Vorbach	Processor Arrangement on a Chip Including Data Processing, Memory, and Interface Elements	Pact XPP Technologies AG	Washington, DC, USA	19 May 2015	http://www.google.com/patents/US9037807

	US 9,047,440	**D**	**1**	**0**		M. Vorbach et al.	Logical Cell Array and Bus System	Pact XPP Technologies AG	Washington, DC, USA	2 Jun. 2015	http://www.google.com/patents/US9047440
39.00			**39**	**0**	**0.00**						
P011	**US 6,580,296**					**V. Beiu**	**Low-Power Differential Conductance-Based Logic Gate and Method of Operation Thereof**	**RN2R**	**Washington, DC, USA**	**17 Jun. 2003**	**1 - 18**
	spie	**D**	**1**	**0**		M. Mirhassani et al.	16-bit Radix-4 Continuous Valued Digit Adder	Proceedings SPIE	San Diego, CA, USA	13-17 Aug. 2006	631303 (1 - 12)
	ACSSC-06	**C**	**2**	**0**		M. Mirhassani et al.	16-bit Binary Multiplication Using High Radix Analog Digits	IEEE Asilomar Conference on Signals, Systems and Computers	Pacific Grove, CA, USA	29 Oct. - 1 Nov. 2006	332 - 336
	ISCAS-07	**C**	**2**	**0**		M. Mirhassani et al.	Digital Multiplication using Continuous Valued Digits	IEEE International Symposium on Circuits and Systems	New Orleans, LA, USA	27-30 May. 2007	3263 - 3266
	PhD	**D**	**1**	**0**		M. Mirhassani	Computer Arithmetic Based on the Continous Valued Number System	University of Windsor	Winsor, ON, Canada	2007	1 - 147
	US 7,183,795	**D**	**1**	**0**		Y. Ye et al.	Majority Voter Apparatus, Systems, and Methods	Intel	Washington, DC, USA	27 Feb. 2007	1 - 9
	US 7,236,005	**D**	**1**	**0**		Y. Ye et al.	Majority Voter Circuit Design	Intel	Washington, DC, USA	26 Jun. 2007	1 - 8
	US 8,164,359	**D**	**1**	**0**		S. Leshner and S. Vrudhula	Threshold Logic Element Having Low Leakage Power and High Performance	Arizona State University	Washington, DC, USA	24 Apr. 2012	1 - 18
	US 8,526,601	**D**	**1**	**0**		A. Garg and S.-K. Lai	Method of Improving Operational Speed of Encryption Engine	AMD	Washington, DC, USA	Sept. 2013	1 - 14
	US 8,767,483	**D**	**1**	**0**		J.M. Brown and V. Bringivijayaraghavan	Apparatus and Methods Having Majority Bit Detection	Micron Technology, Inc.	Washington, DC, USA	1 Jul. 2014	1 - 23
	US 8,832,614	**D**	**1**	**0**		S. Vrudhula and N. Kulkarni	Technology Mapping for Threshold and Logic Gate Hybrid Circuits	Arizona State University	Washington, DC, USA	9 Sept. 2014	1 - 27
12.00			**12**	**0**	**0.00**						
T032	**LA-UR-97-483**					**S. Draghici, and V. Beiu**	**Entropy Based Comparison of Neural Networks for Classification**	**Los Alamos Unrestricted Report LA-UR-97-483**	**Los Alamos, NM, USA**	**1997**	
	springer	**D**	**1**	**0**		S. Draghici	On the Complexity of VLSI-friendly Neural Networks for Classification Problems	Biennial Conference of the Canadian Society for Computational Studies of Intelligence (LNCS 1418)	Vancouver, Canada	18-20 Jun. 1998	285 - 297
1.00			**1**	**0**	**0.00**						
Tu07	**NGCM-04**					**V. Beiu, and S. Roy**	**Practical Redundant Designs for Nano Architectures – Novel Theoretical Results**	**International Symposium on Nano and Giga Challenges in Nanoelectronics**	**Krakow, Poland**	**17 Sept. 2004**	
	Journal	**B**	**4**	**4**		A. Mukati	A Survey of Memory Error Correcting Techniques for Improved Reliability	**Journal of Network and Computer Applications**	Vol. 34, No. 2	Mar. 2010	517 - 522
4.00			**4**	**4**	**4.00**						
2674.45					**1996.53**						

	Carti (editate) si capitole					All are based on the WASS-SENSE book publishers ranking list 2015 (no ranking before 2007)					
	Ch01	A	8	8		V. Beiu	Optimal VLSI Implementations of Neural Networks	In J.G. Taylor (Ed.): Neural Networks and Their Applications	John Wiley & Sons	1996	255 - 276
	Ch02	A	8	8		V. Beiu	Digital Integrated Circuit Implementations (of Neural Networks)	In E. Fiesler, and R. Beale (Eds.): Handbook of Neural Computations	Oxford Univ Press	1996	E1.4. 1 - 34
	Ch03	B	4	4		V. Beiu	Constant Fan-in Discrete Neural Networks Are VLSI-Optimal	In S.W. Ellacott, J.C. Mason, and I.J. Anderson (Eds.): Mathematics of Neural Networks Models, Algorithms and Applications	Kluwer Academic	1997	89 - 94
	Ch04	–	1	1		V. Beiu	Entropy, Constructive Neural Learning, and VLSI Efficiency	In R. Andonie, and D. Grosu (Eds.): Neural Priorities in Data Transmission and EDA	"Transilvania" Univ. Press	1998	38 - 74
	Ch05	B	4	4		V. Beiu, and W. Ibrahim	On Computing Nano-Architectures Using Unreliable Nano-Devices	In S.E. Lyshevski (Ed.): Nano- and Molecular-Electronics Handbook	CRC Press / Taylor & Francis Group	2007	12. 1 - 49
	Ch06	–	1	1		V. Beiu, W. Ibrahim, and S. Lazarova-Molnar	On Device-level Majority von Neumann Multiplexing	In J.R. Rabuñal et al. (Eds.): Encyclopedia of Artificial Intelligence	IGI Global	2009	471 - 479
	Ch07	B	4	2		A. Beg, M.H. Sulieman, V. Beiu, and W. Ibrahim	Low-Power Reliable Nano Adders	In J.E. Morris and K. Iniewski (Eds.): Nanoelectronic Device Applications Handbook	CRC Press / Taylor & Francis Group	2013	67 - 75
	Ch08	B	4	2		V. Beiu, L. Zhang, A. Beg, W. Ibrahim, and M. Tache	Axon-Inspired Communication Systems	In J.E. Morris and K. Iniewski (Eds.): Nanoelectronic Device Applications Handbook	CRC Press / Taylor & Francis Group	2013	193 - 208
30.00				30.00							

	Editor proceedings										
	Springer	D	1	0.33		A. Schmid, S. Goel, W. Wang, V. Beiu, and S. Carrara (Eds.)	Nano-Net (International ICST Conference, NanoNet'08) Revised Selected Papers	ISBN 978-3-642-02427-6	Springer LNICS	Oct. 2009	
	IEEE	D	1	1		V. Beiu, and S. Harous (Eds.)	Innovations	ISBN 978-1-4799-7212-8	IEEE Press	Nov. 2014	
1.33				1.33							

	Curs universitar in format electronic									
				2			ASIC & Digital Systems	Washington State University & United Arab Emirates University	Pullman, WA, USA	2001 - 2015	
				2			Advanced VLSI/Nanoelectronics	Washington State University	Pullman, WA, USA	2004, 2005	
				2			Hardware Testing and Fault Tolerance	United Arab Emirates University	Al Ain, UAE	2013 - 2015	
				2			Professional Responsibility in IT	United Arab Emirates University	Al Ain, UAE	2012 - 2015	

				2			Research Methods in IT	United Arab Emirates University	Al Ain, UAE	2011 - 2013	
				2			Neuro-Bio Fundamentals	"Aurel Vlaicu" University of Arad	Arad, Romania	2015	
				2			Neural Computations	"Aurel Vlaicu" University of Arad	Arad, Romania	2016	
14.00				14.00							
	Director/editor al unei reviste										
		A		24			Associate Editor	IEEE Transactions on Neural Networks	IEEE	2005 - 2008	
		B		12			Associate Editor	Nano Communication Networks	Elsevier	2010 - 2015	
		B		12			Associate Editor	IEEE Transactions on VLSI Systems	IEEE	2011 - 2015	
48.00				48.00							
	Director/membru al unui grant/proiect/contract de cercetare										
	Director	> 200K€		8			Novel Bio-inspired Cellular Nano-Architectures (BioCell-NanoART)	ANCSI/MFE -- POC-A1-A1.1.3-E-2015	8.5M RON	2016 - 2019	
	Director	~100K€		6			Ultra-low Power Digital Sub-threshold FinFET Amplifiers (ULP-DigiFinA)	Semiconductor Research Corporation (SRC) -- GRC ACE4S	120K$	2014 - 2015	
	Director	> 200K€		8			Ultra Low Power NEMS-CMOS (ULP-NEMS-CMOS)	Semiconductor Research Corporation (SRC) -- 2011-HJ-2184	300K$	2011 - 2015	
	Director	>100K€		6			Unconventional Sizing for Enabling Low Power Digital Design (Use-LP)	Semiconductor Research Corporation (SRC) -- 2012-TJ-2332	200K$	2012 - 2014	
	Director	>100K€		6			Brain-inspired Interconnects for Nanoelectronics (BiIN)	National Research Foundation (NRF) -- 1108-00451	160K$	2011 - 2013	
	Director	<50K€		2			Brain-inspired Hybrid Topologies for Nano-architectures	Semiconductor Research Corporation (SRC) -- 2011-RJ-2150G	40K$	2011 - 2012	
	Director	~50K€		4			Brain-inspired Interconnects for Nanoelectronics	British Council -- PMI2 RCGS271	39K£	2009 - 2011	
	Director	> 200K€		8			Ultra-fast Low-power FPUs for Graphics and Gaming	Rose Research	500K$	2000 - 2003	
	Director	> 200K€		8			Ultra-fast Low-power En/decryption for Wire-speed Crypto-processors	Rose Research	500K$	2000 - 2003	
	Director	> 200K€		8			FastLogic (enabling VLSI based on novel ultra-fast logic gates)	Rose Research	3M$	1999 - 2005	
	Director	> 200K€		8			Ultra-fast Low-power Multiplication & Multiply-accumulate for DSP	Rose Research	1M$	1999 - 2002	
	Director	> 200K€		8			Enhanced Ultra-fast VLSI Adders	Rose Research	500K$	1998 - 1999	
	Director	>100K€		6			Field Programmable Neural Arrays	Los Alamos National Laboratory	180K$	1996 - 1998	
	Director	> 200K€		8			Programmable Neural Arrays for Implementing Neural Networks	European Union -- CHBICT941741	440K$	1994 - 1996	
	Director	<50K€		2			Dedicated En/Decryption and GUI	Ministry of National Defense	~20K$	1990 - 1991	
	Director	<50K€		2			Computer Aided Designing	Aversa SA	~5K$	1990 - 1991	
	Director	<50K€		2			Data Acquisition CAD Package	Chemistry Research Institute	~10K$	1990 - 1991	
	Director	<50K€		2			Dedicated/Custom Software Package	Ministry of National Defense	~5K$	1990 - 1991	
	Director	<50K€		2			Dedicated Watch-dog System	Electrical Networks Institute	~50K$	1988	
	Director	<50K€		2			Dedicated Database Package	National Institute for Information & Documentation	~50K$	1987	
	Director	<50K€		2			Hierarchical Self-testable/-repairable Content Addressable Memory	University "Politehnica" of Bucharest	~50K$	1987	
	Director	>50K€		4			High Speed Antialiasing Cascadable Circuit	University "Politehnica" of Bucharest	~50K$	1987	
	Director	>50K€		4			VLSI CAD Package	University "Politehnica" of Bucharest	~100K$	1985 - 1987	
	Director	>50K€		4			Automatic Conical Ball Bearing Sorter	Rulmentul Alexandria (now Koyo)	~100K$	1984 - 1986	
	Director	<50K€		2			Mutual exclusion circuit (patented)	Centrul de Cercetari pentru Automatica Bucharest	Not known	1983	
	Director	<50K€		2			Ultra high-speed highly reliable CPU	Centrul de Cercetari pentru Automatica Bucharest	Not known	1981	
	Director	<50K€		2			High speed (60MHz) graphic workstation (1024×1024)	University "Politehnica" of Bucharest	~5K$	1979 - 1980	

	Director					93 short-term travel grants	Various agencies/universties/labs (see CV)	~227K$	1987 - ……	
	Member	> 200K€	4			Strengthening Research Collaborations in High-impact & Emerging Technologies between GCC and EU (SECRET)	European Union -- EM 545790-EM-1-2013-1-UK-ERA MUNDUS-EMA22	1.2M€	2013 - 2016	
	Member	>100K€	3			Ultra Low-Power Application-specific Non-Boolean Architectures (ULP-NBA)	Intel -- URO 2011-05-24G	1M$	2011 - ……	
	Member	<50K€	1			Synaptic Molecular Networks for Bio-inspired Information Processing	European Union -- FP7-ICT-318597	2.8M€	2012 - 2015	
	Member	>100K€	3			Algorithms & EDA for Accurate Nano-Circuits Reliability Calculations	National Research Foundation (NRF) -- 1108-00329	138K$	2011 - 2013	
	Member	> 200K€	4			Emirates Center for Nanoscience & Nanoengineering (on hold)	National Research Foundation (NRF)	13.6M$	2009 - ……	
	Member	> 200K€	4			Center for Neural Inspired Nano Architectures	University of Ulster / Center for Excellence in Intelligent Systems	1.8M£	2007 - 2010	
	Member	<50K€	1			Mapping the Proxel Method to Reliability Analysis of Nanoarchitectures	United Arab Emirates University (internal grant)	2K$	2007	
	Member	> 200K€	4			Center for Excellence in Intelligent Systems	InvestNI & IDF	20.4M£	2006 - ……	
	Member	<50K€	1			Investigation of the reliability of SET gates & circuits	United Arab Emirates University (internal grant)	2K$	2006	
	Member	>50K€	2			Defect-tolerant high-performance low-power computing with hybrid CMOL	Advanced Research and Development Activity (later Disruptive Technology Office and now Intelligence Advanced Research Projects Activity)	100K$	2005 - 2006	
	Member	> 200K€	4			DDFS's for reconfigurable communication system	Air Force Research Laboratory (AFRL)	250K$	2002 - 2004	
	Member	<50K€	1			VLSI-efficient threshold logic gates	Concerted Research Action of the Flemish Community	~20K$	1992 - 1994	
	Member	<50K€	1			Software Package for Microbusiness	National Institute of Research & Development in Chemistry & Petrochemistry	~10K$	1990 - 1991	
	Member	<50K€	1			Studies and Analyzes of Prolog as a Tool for Circuit Simulations	University "Politehnica" of Bucharest	Not known	1987 - 1988	
	Member	<50K€	1			Floppy disk interface	Centrul de Cercetari pentru Automatica Bucharest	Not known	1983	
	Member	<50K€	1			Testing of the CE-100 computer	Centrul de Cercetari pentru Automatica Bucharest	Not known	1980	
162.00			**162.00**							

Membru in comitetul stiintific (de program) al unor conferinte										
	RRCS-94	**D**	1	**1**			TPC (Technical Program Committee) member	International Conference Romania and Romanians in Contemporary Science	Sinaia, Romania	24-27 May 1994
	ANITA-96	–	0	**0**			TPC (Technical Program Committee) member	Shaping the Hardware Solutions for the Third Millennium	Uppsala, Sweden	9-10 Dec. 1996
	NEuroFuzzy-96	–	0	**0**			TPC (Technical Program Committee) member	IEEE International Symposium on Neuro-Fuzzy Systems	Lausanne, Switzerland	29-31 Aug. 1996
	NeuroTop-97	–	0	**0**			TPC (Technical Program Committee) member	International Workshop on Neural Research Priorities	Brasov, Romania	27-28 May 1997
	SBRN-97	**D**	1	**1**			TPC (Technical Program Committee) member	IEEE Brazilian Symposium on Neural Networks	Goiania, Brazil	3-5 Dec. 1997
	EIS-98	–	0	**0**			TPC (Technical Program Committee) member	International ICSC Symposium on Engineering of Intelligent Systems	Tenerife, Spain	11-13 Feb. 1998
	SOCO-99	–	0	**0**			TPC (Technical Program Committee) member	International Symposium on Soft Computing	Genova, Italy	1-4 June 1999
	EIS-00	–	0	**0**			TPC (Technical Program Committee) member	International ICSC Symposium on Engineering of Intelligent Systems	Paisley, Scotland, UK	27-30 Jun. 2000
	SBRN-00	**D**	1	**1**			TPC (Technical Program Committee) member	IEEE Brazilian Symposium on Neural Networks	Rio de Janiero, Brazil	22-25 Nov. 2000

IWANN-03	**B**	4	**4**		TPC (Technical Program Committee) member	International Work-Conference on Artificial Neural Networks	Menorca, Spain	3-6 Jun. 2003	
NCI-03	**–**	0	**0**		TPC (Technical Program Committee) member	Neural Networks and Computational Intelligence	Cancun, Mexico	19-21 May 2003	
IJCNN-04	**A**	8	**8**		TPC (Technical Program Committee) member	IEEE International Joint Conference on Neural Networks	Budapest, Hungary	25-29 Jul. 2004	
IJCNN-05	**A**	8	**8**		TPC (Technical Program Committee) member	IEEE International Joint Conference on Neural Networks	Montréal, Canada	31 July - 4 Aug. 2005	
NanoArch-05	**–**	0	**0**		TPC (Technical Program Committee) member	International Symposium on Nanoscale Architectures	Palm Springs, CA, USA	1-May-05	
ICMENS-06	**D**	1	**1**		TPC (Technical Program Committee) member	International Conference on MEMS, NANO and Smart Systems (DBLP)	Cairo, Egypt	27-29 Dec. 2006	
IDT-06	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE International Design and Test Workshop	Dubai, UAE	19-20 Nov. 2006	
IEEE-NANO-06	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE International Nanotechnolgy Conference	Cincinnati, Ohio, USA	17-20 Jun. 2006	
IEEE SoC-06	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE System-on-Chip Conference	Austin, TX, USA	24-27 Sept. 2006	
IJCNN-06	**A**	8	**8**		TPC (Technical Program Committee) member	IEEE International Joint Conference on Neural Networks	Vancouver, BC, Canada	16-21 Jul. 2006	
NanoArch-06	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE/ACM International Symposium on Nanoscale Architectures	Boston, MA, USA	17 Jun. 2006	
WSC-11	**–**	0	**0**		TPC (Technical Program Committee) member	Online World Conference on Soft Computing in Industrial Applications	Online	18 Sept. - 6 Oct. 2006	
IDT-07	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE International Design and Test Workshop	Cairo, Egypt	16-18 Dec. 2007	
IIT-07	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE Innovations in IT	Dubai, UAE	18-20 Nov. 2007	
IEEE SoC-07	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE System-on-Chip Conference	Hsin Chu, Taiwan	26-29 Sep. 2007	
IJCNN-07	**A**	8	**8**		TPC (Technical Program Committee) member	IEEE International Joint Conference on Neural Networks	Orlando, FL, USA	12-17 Aug. 2007	
MCSoC-07	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE International Symposium on Embedded Multicore/Many-core Systems-on-Chip	XiAn, China	10-14 Sept. 2007	
NanoArch-07	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE/ACM International Symposium on Nanoscale Architectures	San Jose, CA, USA	21-22 Oct. 2007	
WSC-12	**–**	0	**0**		TPC (Technical Program Committee) member	Online World Conference on Soft Computing in Industrial Applications	Online	16-26 Oct. 2007	
IDT-08	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE International Design and Test Workshop	Monastir, Tunisia	20-22 Dec. 2008	
MIM-MMN-08	**–**	0	**0**		TPC (Technical Program Committee) member	National Conference on Mechatronics, Mechanical Engineering, Microtechnology and New Materials	Targoviste, Romania	7 Nov. 2008	
NanoArch-08	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE/ACM International Symposium on Nanoscale Architectures	Anaheim, CA, USA	12-13 Jun. 2008	
NDCS-08	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE International Workshop on Design and Test of Nano Devices, Circuits and Systems	Cambridge, MA, USA	29-30 Sept. 2008	
VTS-08	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE VLSI Test Symposium	San Diego, CA, USA	27 Apr. - 1 May 2008	

WSC-13	–	0	0		TPC (Technical Program Committee) member	Online World Conference on Soft Computing in Industrial Applications	Online	10-28 Nov. 2008	
DTIS-09	**D**	1	1		TPC (Technical Program Committee) member	IEEE International Conference on Design & Technology of Integrated Systems in Nanoscale Era	Cairo, Egypt	6-7 Apr. 2009	
ICMLA-09	**C**	2	2		TPC (Technical Program Committee) member	International Conference on Machine Learning	Miami, FL, USA	13-15 Dec. 2009	
IJCNN-09	**A**	8	8		TPC (Technical Program Committee) member	IEEE International Joint Conference on Neural Networks	Atlanta, GA, USA	14-19 Jun. 2009	
MIM-MMN-09	–	0	0		TPC (Technical Program Committee) member	National Conference on Mechatronics, Mechanical Engineering, Microtechnology and New Materials	Targoviste, Romania	19 Jun. 2009	
NanoArch-09	**D**	1	1		TPC (Technical Program Committee) member	IEEE/ACM International Symposium on Nanoscale Architectures	San Francisco, CA, USA	30-31 Jul. 2009	
NanoNet-09	**D**	1	1		TPC (Technical Program Committee) member	International ICST Conference on Nano-Networks (Springer)	Luzern, Switzerland	18-20 Oct. 2009	
WSC-14	–	0	0		TPC (Technical Program Committee) member	Online World Conference on Soft Computing in Industrial Applications	Online	17-29 Nov. 2009	
BIONETICS-10	–	0	0		TPC (Technical Program Committee) member	International Conference on Bio-Inspired Models of Network, Information and Computing Systems	Boston, MA, USA	1-3 Dec. 2010	
ICTITA-10	–	0	0		TPC (Technical Program Committee) member	International Conference on Trends in Information Technology and Applications	Ajman, UAE	11-13 Dec. 2010	
IDT-10	**D**	1	1		TPC (Technical Program Committee) member	IEEE International Design and Test Workshop	Abu Dhabi, UAE	14-15 Dec. 2010	
MIM-MM-10	–	0	0		TPC (Technical Program Committee) member	National Conference on Mechatronics, Mechanical Engineering, Microtechnology and New Materials	Targoviste, Romania	18 Jun. 2010	
MCSoC-10	**D**	1	1		TPC (Technical Program Committee) member	IEEE International Symposium on Embedded Multicore SoCs	San Diego, CA, USA	13-16 Sept. 2010	
NanoArch-10	**D**	1	1		TPC (Technical Program Committee) member	IEEE/ACM International Symposium on Nanoscale Architectures	Anaheim, CA, USA	17-18 Jun. 2010	
NanoNet-10	–	0	0		TPC (Technical Program Committee) member	ICPC Nanonet Annual Workshop	Beijing, China	14-15 Jun. 2010	
SBCCI-10	**D**	1	1		TPC (Technical Program Committee) member	IEEE Symposium on Integrated Circuits and Systems Design	Sao Paulo, Brazil	6-9 Sept. 2010	
WAC-10	**D**	1	1		TPC (Technical Program Committee) member	IEEE World Automation Congress	Kobe, Japan	19-23 Sept. 2010	
WSC-15	–	0	0		TPC (Technical Program Committee) member	Online World Conference on Soft Computing in Industrial Applications	Online	15-27 Nov. 2010	
ICMLA-11	**C**	2	2		TPC (Technical Program Committee) member	International Conference on Machine Learning	Honolulu, Hawaii	18-21 Dec. 2011	
IDT-11	**D**	1	1		TPC (Technical Program Committee) member	IEEE International Design and Test Workshop	Beirut, Lebanon	11-14 Dec. 2011	
MIM-MMN-11	–	0	0		TPC (Technical Program Committee) member	National Conference on Mechatronics, Mechanical Engineering, Microtechnology and New Materials	Targoviste, Romania	10 Jun. 2011	
MoNaCom-11	**D**	1	1		TPC (Technical Program Committee) member	IEEE International Workshop on Molecular and Nano Scale Communication	Shanghai, China	10-15 Apr. 2011	
NaBIC-11	–	0	0		TPC (Technical Program Committee) member	World Congress on Nature and Biologically Inspired Computing	Salamanca, Spain	19-21 Oct. 2011	
NanoArch-11	**D**	1	1		TPC (Technical Program Committee) member	IEEE/ACM International Symposium on Nanoscale Architectures	Salamanca, Spain	19-21 Oct. 2011	

SBCCI-11	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE Symposium on Integrated Circuits and Systems Design	João Pessoa, Brazil	6-9 Sep. 2011	
ISIE-12	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE International Symposium on Industrial Electronics	Gdansk, Poland	27-30 Jun. 2011	
MIM-MMN-12	–	0	**0**		TPC (Technical Program Committee) member	National Conference on Mechatronics, Mechanical Engineering, Microtechnology and New Materials	Targoviste, Romania	10 Jun. 2011	
MoNaCom-12	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE International Workshop on Molecular and Nano Scale Communication	Ottawa, Canada	10-15 Jun. 2012	
NaBIC-12	–	0	**0**		TPC (Technical Program Committee) member	World Congress on Nature and Biologically Inspired Computing	Mexico City, Mexico	5-9 Nov. 2012	
NanoArch-12	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE/ACM International Symposium on Nanoscale Architectures	Amsterdam, Netherlands	4-6 Jul. 2012	
OPTIM-12	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE International Conference on Optimization of Electrical and Electronic Equipment	Brasov, Romania	24-26 May 2012	
SBCCI-12	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE Symposium on Integrated Circuits and Systems Design	Brasilia, Brazil	30 Aug. - 2 Sep. 2012	
WICT-12	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE World Congress on Information and Communication Technologies	Trivandrum, India	30 Oct. - 2 Nov. 2012	
WSC-16	–	0	**0**		TPC (Technical Program Committee) member	Online World Conference on Soft Computing in Industrial Applications	Online	5-16 Dec. 2011	
DTIS-13	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE International Conference on Design & Technology of Integrated Systems in Nanoscale Era	Abu Dhabi, UAE	26-28 Mar. 2013	
ICECS-13	**D**	1	**1**	**Track Chair**		IEEE International Conference on Electronics, Circuits, and Systems	Abu Dhabi, UAE	8-11 Dec. 2013	
IDT-13	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE International Design and Test Workshop	Marrakesh, Morocco	16-18 Dec. 2013	
IIT-13	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE Innovations in IT	Al Ain, UAE	17-19 Mar. 2013	
IJCNN-13	**A**	8	**8**		TPC (Technical Program Committee) member	IEEE International Joint Conference on Neural Networks	Dallas, TX, USA	4-9 Aug. 2013	
MIM-MMN-13	–	0	**0**		TPC (Technical Program Committee) member	National Conference on Mechatronics, Mechanical Engineering, Microtechnology and New Materials	Targoviste, Romania	21 Jun. 2013	
MoNaCom-13	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE International Workshop on Molecular and Nano Scale Communication	Budapest, Hungary	9-13 Jun. 2013	
NanoArch-13	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE/ACM International Symposium on Nanoscale Architectures	Brooklyn, NY, USA	15-17 Jul. 2013	
SBCCI-13	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE Symposium on Integrated Circuits and Systems Design	Curitiba, Brazil	2-6 Sept. 2013	
VLSI-SoC-13	**D**	1	**1**		TPC (Technical Program Committee) member	IFIP/IEEE International Conference on Very Large Scale Integration	Istanbul, Turkey	6-9 Oct. 2013	
BICT-14	–	0	**0**		TPC (Technical Program Committee) member	International Conference on Bio-inspired Information and Communications Technologies	Boston, MA, USA	1-3 Dec. 2014	
BioTL-14	–	0	**0**		TPC (Technical Program Committee) member	Symposium on Biomorphic Circuits and Systems with Threshold Logic	Boston, MA, USA	7-9 Nov. 2014	
DTIS-14	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE International Conference on Design & Technology of Integrated Systems in Nanoscale Era	Santorini, Greece	6-8 May 2014	
I4CT-14	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE International Conference on Computer, Communication and Control Technology	Kedah, Malaysia	2-4 Sept. 2014	

ICECS-14	**D**	1	**1**	**Track Chair**		IEEE International Conference on Electronics, Circuits, and Systems	Marseille, France	7-10 Dec. 2014	
ICNC-14	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE International Conference on Computing, Networking and Communications	Honolulu, HI, USA	3-6 Feb. 2014	
IIT-14	**D**	1	**1**	**Chair**		IEEE Innovations in IT	Al Ain, UAE	9-11 Nov. 2014	
IDT-14	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE International Design and Test Workshop	Algeries, Algeria	16-18 Dec. 2014	
ISCAS-14	**C**	2	**2**		TPC (Technical Program Committee) member	IEEE International Symposium on Circuits and Systems	Melbourne, Australia	1-5 Jun. 2014	
MIM-MMN-14	**–**	0	**0**		TPC (Technical Program Committee) member	National Conference on Mechatronics, Mechanical Engineering, Microtechnology and New Materials	Targoviste, Romania	27 Jun. 2014	
NanoArch-14	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE/ACM International Symposium on Nanoscale Architectures	Paris, France	8-10 Jul. 2014	
NanoCom-14	**D**	1	**1**		TPC (Technical Program Committee) member	ACM International Conference on Nanoscale Computing and Communication	Atlanta, GA, USA	13-14 May 2014	
SBCCI-14	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE Symposium on Integrated Circuits and Systems Design	Aracaju, Brazil	1-5 Sept. 2014	
SSCI-14	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE Symposium Series on Computational Intelligence	Orlando, FL, USA	9-12 Dec. 2014	
DTIS-15	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE International Conference on Design & Technology of Integrated Systems in Nanoscale Era	Napoli, Italy	21-23 Apr. 2015	
ECCTD-15	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE European Conference on Circuit Theory and Design	Trondheim, Norway	24-26 Aug. 2015	
ICECS-15	**D**	1	**1**	**Track Chair**		IEEE International Conference on Electronics, Circuits, and Systems	Cairo, Egypt	6-9 Dec. 2015	
IDT-15	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE International Design and Test Workshop	Dead Sea, Jordan	14-16 Dec. 2015	
IJCNN-15	**A**	8	**8**		TPC (Technical Program Committee) member	IEEE International Joint Conference on Neural Networks	Killarney, Ireland	12-17 Jul. 2015	
MIM-MMN-15	**–**	0	**0**		TPC (Technical Program Committee) member	National Conference on Mechatronics, Mechanical Engineering, Microtechnology and New Materials	Targoviste, Romania	26 Jun. 2015	
NaBIC-15	**–**	0	**0**		TPC (Technical Program Committee) member	World Congress on Nature and Biologically Inspired Computing	Pietermaritzburg, South Africa	1-3 Dec. 2015	
NanoArch-15	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE/ACM International Symposium on Nanoscale Architectures	Boston, MA, USA	8-10 Jul. 2015	
NanoCom-15	**D**	1	**1**		TPC (Technical Program Committee) member	ACM International Conference on Nanoscale Computing and Communication	Boston, MA, USA	21-22 Sept. 2015	
SBCCI-15	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE Symposium on Integrated Circuits and Systems Design	Salvador, Brazil	31 Aug. - 4 Sep. 2015	
SSCI-15	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE Symposium Series on Computational Intelligence	Cape Town, South Africa	7-10 Dec. 2015	
DTIS-16	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE International Conference on Design & Technology of Integrated Systems in Nanoscale Era	Napoli, Italy	21-23 Apr. 2015	
ICCCC-16	**D**	1	**1**		TPC (Technical Program Committee) member	IEEE International Conference on Computers, Communications and Control	Baile Felix, Oradea, Romania	10-14 May 2016	
ICECS-16	**D**	1	**1**	**Publicity Chair**		IEEE International Conference on Electronics, Circuits, and Systems	Monte Carlo, Monaco	11-14 Dec. 2016	

	IDT-16	**D**	1	**1**			TPC (Technical Program Committee) member	IEEE International Design and Test Workshop	Hammamet, Tunisia	18-20 Dec. 2016	
	ISCAS-16	**C**	2	**2**			TPC (Technical Program Committee) member	IEEE International Symposium on Circuits and Systems	Montreal, Canada	22-25 May 2016	
	MIM-MMN-16	–	0	**0**			TPC (Technical Program Committee) member	National Conference on Mechatronics, Mechanical Engineering, Microtechnology and New Materials	Targoviste, Romania	21 Jun. 2016	
	SOFA-16	**C**	2	**2**			TPC (Technical Program Committee) member	International Workshop on Soft Computing Applications	Arad, Romania	24-26 Aug. 2016	
	SETIT-16	**D**	1	**1**			TPC (Technical Program Committee) member	IEEE International Conference on Sciences of Electronics, Technologies of Information and Telecommunications	Hammamet, Tunisia	18-20 Dec. 2016	
	ISCAS-17	**C**	2	**2**			TPC (Technical Program Committee) member	IEEE International Symposium on Circuits and Systems	Baltimore, MD, USA	28-31 May 2017	
	DTIS-17	**D**	1	**1**			TPC (Technical Program Committee) member	IEEE International Conference on Design & Technology of Integrated Systems in Nanoscale Era	Palma de Mallorca, Spain	4-6 Apr. 2017	
139.00				**139.00**							

	Organizarea de evenimente stiintifice										
				1		V. Beiu, and R. Andonie	Shaping the Hardware Solutions for the Third Millennium	Invited workshop ANITA'96	Uppsala, Sweden	9-10 Dec. 1996	
				1		R. Andonie, and V. Beiu	Neural Research Priorities	Invited workshop NeuroTop'97	Braşov, Romania	27-28 May 1997	
				2		V. Beiu	The Next Generation of Neural Networks Chips	Invited session at the International ICSC Symposium on Engineering of Intelligent Systems EIS'98	Tenerife, Spain	9 Feb. 1998	
				2		V. Beiu	Threshold Gates – Past, Present, and Future	Invited session at the International Work-Conference on Artificial Neural Networks IWANN'03	Menorca, Spain	4 Jun. 2003	
				2		V. Beiu, and U. Rückert	Neural-inspired Architectures for Nanoelectronics	Invited workshop at Neural Information Processing Systems NIPS'03	Whistler, Canada	12-13 Dec. 2003	
				2		V. Beiu, and U. Rückert	Brain Inspired Emerging Nanoarchitectural Design and Technical Challenges	Invited session at the IEEE International Joint Conference on Neural Networks IJCNN'04	Budapest, Hungary	28 Jul. 2004	
				1		U. Rückert, and V. Beiu	Neural Inspired Architectures for Nanoelectronics	Invited session at the International Work-Conference on Artificial Neural Networks IWANN'07	San Sebastian, Spain	19 May 2007	
				1		M.J. Avedillo, J.M. Quintana, and V. Beiu	Emerging Technologies Applied to Nanoelectronics	Invited session at the International Conference on Design of Circuits and Integrated Systems DCIS'07	Seville, Spain	22 Nov. 2007	
				2		V. Beiu, and W. Ibrahim	Towards Brain Inspired Interconnects and Circuits	Invited worksop at the International ICST Conference on Nano-Networks Nano-Net'09	Luzern, Switzerland	18 Oct. 2009	
				1		R. Andonie, D. Davendra, and V. Beiu	Computational Intelligence Methods	Invited session at the IEEE International Conference on Computers, Communications and Control ICCCC'16	Baile Felix, Oradea, Romania	12 May 2016	
15.00				**15.00**							

	Keynote/invited speaker										
		B	4	**4**		V. Beiu	How to Build VLSI-Efficient Neural Chips	International ICSC Symposium on Engineering of Intelligent Systems EIS'98	Tenerife, Spain	11 Feb. 1998	
		B	4	**4**		V. Beiu	Neural Inspired Parallel Computations Require Analog Processors	International Conference on Parallel Computing and Electrical Engineering PARELEC'98	Bialystok, Poland	4 Sept. 1998	
		B	4	**4**		V. Beiu	2D Neural Hardware vs 3D Biological Ones	International ICSC Symposium on Neural Computations NC'98	Vienna, Austria	22 Sept. 1998	

	B	4	**4**		V. Beiu	On Biological and Hardware Neural Networks	International Joint Meeting of the AMS and SMM	Denton, TX, USA	21 May 1999	
	B	4	**4**		U. Rükert, and V. Beiu	Neural Inspired Architectures for Nanoelectronics	IEEE International Conference on Intelligent Computing and Information Systems ICICIS'05	Cairo, Egypt	5-7 Mar. 2005	
	B	4	**4**		V. Beiu	The Quest for Reliable Nano Computations	IEEE International Conference on Microelectronics ICM'05	Islamabad, Pakistan	13 Dec. 2005	
	B	4	**4**		V. Beiu	What Do Moore, von Neumann and Kolmogorov Have in Common?	IEEE International Conference on Computer Systems and Applications AICCSA'06	Sharjah, UAE	9 Mar. 2006	
	B	4	**4**		V. Beiu	What Do Shannon, von Neumann, Kolmogorov, and Feynman Have to Do with ... Moore?	IEEE International Symposium on Multiple Valued Logic ISMVL'07	Oslo, Norway	14 May 2007	
	B	4	**4**		V. Beiu	Quo Vadis Nano-electronics	Information Electronics Systems Global Center of Excellence GCoE'07 (Tohoku University)	Sendai, Japan	27 Nov. 2007	
	B	4	**1.33**		S. Bhabhu, R.A. Parekhji, M. Nicolaidis, V. Beiu, and M.Y. Zhang	Mitigating Reliability, Yield and Power Issues in Nano-CMOS: Design or EDA Problem?	IEEE International VLSI Test Symposium VTS'08	San Diego, CA, USA	30 Apr. 2008	
	B	4	**4**		V. Beiu	Electrons Behaving Badly	Information Electronics Systems Global Center of Excellence GCoE'08 (Tohoku University)	Sendai, Japan	14 Jul. 2008	
	B	4	**1**		C. Constantinescu, J.A. Abraham, V. Beiu, H. Naeimi, A. Somani, and S. Wang	Scaling Towards Nanometer Size Devices – Issues and Solutions	Workshop on Dependable and Secure Nanocomputing WDSN'09 (IEEE / IFIP DSN'09)	Estoril/Lisbon, Portugal	29 Jun. 2009	
	B	4	**4**		V. Beiu	Connectivity and Scalability Issues for Biologically Plausible Nano-electronic Systems	International Workshop on Brain-Inspired Electronic Circuits and Systems BIECS'09 (European Solid-State Device Research Conference ESSDERC'09)	Athens, Greece	18 Sept. 2009	
	B	4	**4**		V. Beiu	Trustworthy Wings of the Mysterious Butterflies (Brain-inspired Information Processing)	International Nanotechnology Conference on Communication and Cooperation INC6	Grenoble, France	19 May 2010	
	B	4	**1.33**		T.G. Noll, P. Horn, N. Menezes, V. Beiu, and D. Hammerstrom	Alternative Minimum-Energy Computing Paradigms (Brain-inspired Information Processors)	International Forum on Minimum Energy Electronic Systems MEES'10	Abu Dhabi, UAE	24 May 2010	
	B	4	**4**		V. Beiu	On the Reliability Accuracy Challenge — Grappling with a Seemingly Intractable Problem	European Dependable Computing Conference EDCC'12	Sibiu, Romania	11 May 2012	
	B	4	**4**		V. Beiu	Why the Brain Can and the Computer Can't	IEEE International Workshop on Soft Computing Applications SOFA'16	Arad, Romania	25 Aug. 2016	
59.67			**59.67**							

Visiting professor								
	699	**0.25**			1 week	University of Pernambuco	Recife, Brazil	Nov. 1996	
	<100	**2.00**			1 week	Dalle Molle Institute for Perceptual AI (IDIAP) -- Research Institute (does not appear in webometrics)	Martigny, Switzerland	Oct. 1997	
	711	**0.25**			1 week	Heinz Nixdorf Institute / University of Paderborn	Paderborn, Germany	Sept. 1997	

		4	2.00			1 week	Berkeley Wireless Research Center / University of California at Berkeley	Berkeley, CA, USA	Nov. 2001	
		<100	8.00			1 month (4 weeks)	Los Alamos National Laboratory (LANL)	Los Alamos, NM, USA	Jul. 2002	
		711	0.25			1 week	Heinz Nixdorf Institute / University of Paderborn	Paderborn, Germany	Jul. 2003	
		711	0.25			1 week	Heinz Nixdorf Institute / University of Paderborn	Paderborn, Germany	Aug. 2004	
		<100	2.00			1 week	Los Alamos National Laboratory (LANL) -- Research Institute (does not appear in webometrics)	Los Alamos, NM, USA	Apr. 2008	
		657	0.75			3 weeks (2005, 2010, 2011)	University of Ulster	Magee, UK	2005 - 2011	
		154	4.00			1 month (2 weeks in April & 2 weeks in July)	Technical University of Dresden	Dresden, Germany	2013	
		4	4.00			2 weeks (Sept. 2010, Feb. 2011)	University of California at Berkeley	Berkeley, CA, USA	2010 - 2011	
		154				2 months (approved and pending)	Technical University of Dresden	Dresden, Germany	2017	
23.75			23.75							

	Consolidarea de echipe decercetare										
		5	3	15		V. Beiu	S. Roy, J. Nyathi, M. H. Sulieman, S. Tataputi, D. J. Betowski, P. S. Wu, A. Zawadzki	Washington State University	Pullman, WA, USA	2001 - 2005	
	Nano-ART	10	5	50		V. Beiu	W. Ibrahim, A. Beg, M. H. Sulieman, S. Lazarova-Molnar, B. A. M. Madappuram, H. Amer, M. Tache, F. Kharbash, P. Santagati, L. Dauș, S. R. Cowell, P. Paulin	United Arab Emirates University	Al Ain, UAE	2005 - 2015	
65.00				65.00							

	Membru in comisii de evaluare a tezelor de doctorat										
	PhD	657		0.5		P. M. Kelly	Architectural Requirements for Threshold Logic Gates based on Resonant Tunnelling Devices	University of Ulster	UK	2005	1 - 188
	PhD	1972		0		L. M. Sasu	Computational Intelligence Techniques in Data Mining	Transilvania University of Brasov	Romania	2006	1 - 136
	PhD	1423		0		P. W. C. Prasad	Methods for Simplification and Estimation of Digital Circuit Complexities Using Binary Decision Diagrams	Multimedia University	Malaysia	2007	1 - 228
	PhD	86		4		O. Mirmotahari	Robustness and Performance of Ultra Low Voltage High Speed Logic	University of Oslo	Norway	2008	1 - 141
	PhD	86		4		H. Gundersen	Aspects of Balanced Ternary Arithmetics Implemented Using CMOS Recharged Semi-Floating Gate Devices	University of Oslo	Norway	2008	1-124
	PhD	86		4		J. G. Lomsdalen	Multiple Valued Logic and Recharged Semi-Floating Gate Devices	University of Oslo	Norway	2008	1 - 122
	PhD	273		1		M. He	Contribution à l'étude de l'impact des nanotechnologies sur les architectures : Apprentissage d'inspiration neuronale de fonctions logiques pour circuits programmables	Universite Paris-Sud 11	France	2008	1 - 159
	PhD	86		4		M. Azadmehr	Current-Starved Pseudo Floating-Gate Inverter -- A Bi-Directional Circuit Building Block	University of Oslo	Norway	2009	1 - 150
17.50				17.50							

	Brevete de inventii										
	P001			8		V. Beiu	LSI Unit for Mutual Exclusion	RO 84763	Bucharest, Romania	26 Apr. 1984	1 - 12

	P002			8		V. Beiu	Adder and Multiplier Circuits Employing Logic Gates Having Discrete, Weighted Inputs and Methods of Performing Combinatorial Operations Therewith	US 6,205,458 [also as WO/2000/017802 and AU58155/99]	Washington, DC, USA	20 Mar. 2001	1 - 14
	P003			8		V. Beiu	Logic Gate Having Reduced Power Dissipation and Method of Operation Thereof	US 6,259,275	Washington, DC, USA	10 Jul. 2001	1 - 19
	P004			8		V. Beiu	Adder and Multiplier Circuits Employing Logic Gates Having Discrete, Weighted Inputs and Methods of Performing Combinatorial Operations Therewith	TW 481774	Taipei, Taiwan ROC	1 Apr. 2002	1 - 14
	P005			8		V. Beiu	Noise Tolerant Conductance-Based Logic Gate and Methods of Operation and Manufacturing Thereof	TW 483249	Taipei, Taiwan ROC	11 Apr. 2002	1 - 13
	P006			8		V. Beiu	Adder Having Reduced Number of Internal Layers and Method of Operation Thereof	TW 493139	Taipei, Taiwan ROC	1 Jul. 2002	1 - 15
	P007			8		V. Beiu	Noise Tolerant Conductance-Based Logic Gate and Methods of Operation and Manufacturing Thereof	US 6,430,585 [also as WO/2001/024367 and AU76009/00]	Washington, DC, USA	6 Aug. 2002	1 - 16
	P008			8		V. Beiu	Adder Having Reduced Number of Internal Layers and Method of Operation Thereof	US 6,438,572 [also as WO/2001/023992 and AU40251/01]	Washington, DC, USA	20 Aug. 2002	1 - 11
	P009			8		V. Beiu	Adder Circuits Employing Logic Gates Having Discrete Weighted Inputs and a Method of Operation Therewith	US 6,502,120	Washington, DC, USA	31 Dec. 2002	1 - 13
	P010			8		V. Beiu	Microprocessor and a Digital Signal Processor Including Adder and Multiplier Circuits Employing Logic Gates Having Discrete and Weighted Inputs	US 6,516,331	Washington, DC, USA	4 Feb. 2003	1 - 14
	P011			8		V. Beiu	Low-Power Differential Conductance-Based Logic Gate and Method of Operation Thereof	US 6,580,296	Washington, DC, USA	17 Jun. 2003	1 - 18
88.00				**88.00**							

	Dezvoltarea de pachete si instrumente software etc.										
				2		V. Beiu, A. Florea, and S. Georgescu	NeuroSim	University "Politehnica" of Bucharest			
				2		S. Roy and V. Beiu	Majority Multiplexing	Washington State University			
				2		M. H. Sulieman and V. Beiu	SET Circuits Design Package (MATLAB and Simon)	Washington State University			
				2		S. R. Cowell and V. Beiu	Hammock Networks Simulator	United Arab Emirates University and "Aurel Vlaicu" University of Arad			
8.00				**8.00**							

	Pozitii de conducere in organizatii profesionale										
				4			Mubadala Technology (previously ATIC) Advisory Board			2009 - 2015	
				4			ITRS Roadmap for Semiconductors			2003 - 2015	
8.00				**8.00**							

	Premii si alte merite										
							Gold Medal / First Prize	Romanian Physics Olympiad	4 times	1971 - 1975	
							Highest Award (at graduation)	National College of Informatics		1975	
							Best Paper Awards	University “Politehnica” of Bucharest	5 times	1977 - 1980	
							Best MSc Thesis Award	University “Politehnica” of Bucharest		1980	
							Patent Awards	Romania (1), Taiwan (3), USA (7)	11 times	1984 - 2003	
							PhD summa cum laude	Katholieke Universiteit Leuven		1994	

						Senior Member IEEE	IEEE		1996	
						Best Paper Award	IEEE CAS-00		2000	
						US resident under extraordinary ability “VLSI implementations of neural networks”	US Immigration and Naturalization Service (now US Citizenship and Immigration Services)		2001	
						Best Paper Award	UAEU Annual Research Conference		2008	
						Best Excellence in Scholarship Award	United Arab Emirates University		2009	
						Research Affairs Recognition Award	United Arab Emirates University		2009	
						Excellence Award	"Aurel Vlaicu" University of Arad		2016	
0.00			0.00							

679.25