VALERIU BEIU — PUBLICATIONS

OVERVIEW	PUBLISHED	ACCEPTED
BOOKS	2	3
CHAPTERS	8 (7 INVITED)	5
PATENTS	11	
JOURNALS	35 (2 INVITED)	3 (1 INVITED)
CONFERENCES	207 (26 INVITED)	
TOTAL	274 (36 INVITED, 7 BEST PAPER AWARDS)	
OTHER CONFERENCES	51 (7 INVITED, 1 BEST PAPER AWARD)	
TECHNICAL REPORTS	67	

BOOKS 2

– V. Beiu, and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures
Book in progress (contract signed with World Scientific)

– V. Beiu: VLSI Complexity of Discrete Neural Networks
Book in progress (contract signed with Taylor & Francis)

– V. Beiu, R. Andonie, and R. Dogaru: Fundamental Problems of Neural Networks
Book in progress (contract signed with Technical Printing House)

B_2 V. Beiu, and S. Harous (Eds.): Innovations
IEEE Press, November 2014 (ISBN 9781479972128) 1–132
https://ieeexplore.ieee.org/document/6985768/

B_1 A. Schmid, S. Goel, W. Wang, V. Beiu, and S. Carrara (Eds.): Nano-Net
Springer, LNICS, October 2009 (ISBN 9783642024276) 1–286
https://doi.org/10.1007/978-3-642-04850-0

··· V. Beiu: Neural Networks Using Threshold Gates
A Complexity Analysis of Their Area- and Time-Efficient VLSI Implementations
PhD dissertation, Katholieke Universiteit Leuven, Leuven, Belgium
U.D.C. 621.3.04977: 681.3*C13 (x-27-151779-3), May 1994 1–222

CHAPTERS (7 INVITED) 8

– V. Beiu, and W. Ibrahim: On Enabling Redundant Designs for Nano Computations
In V. Beiu, and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures

– V. Beiu, J.M. Quintana, and M.J. Avedillo
Threshold Logic Design and Implementations: From the Early Days into the Nanoera
In V. Beiu, and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures

– M.H. Sulieman, and V. Beiu
From Single Electron Technology (SET) Full Adders to Optimal Practical SET Adders
In V. Beiu, and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures

– V. Beiu, and U. Rückert: Roadmap for Nano Architectures
In V. Beiu, and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures

– J. Nyathi, and V. Beiu: Advanced Techniques for Reducing Power Consumption
In V. Beiu, and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures

Ch_8 V. Beiu, L. Zhang, A. Beg, W. Ibrahim, and M. Tache: Axon-Inspired Communication Systems ***Invited***$_7$
Chapter 15 in J.E. Morris and K. Iniewski (Eds.): Nanoelectronic Device Applications Handbook, CRC/Taylor & Francis (UK/USA), 2013 (ISBN 9781466565234) 193–208

Ch_7 A. Beg, M.H. Sulieman, V. Beiu, and W. Ibrahim: Low-Power Reliable Nano Adders ***Invited***$_6$
Chapter 6 in J.E. Morris and K. Iniewski (Eds.): Nanoelectronic Device Applications Handbook, CRC/Taylor & Francis (UK/USA), 2013 (ISBN 9781466565234) 67–75

Ch_6 V. Beiu, W. Ibrahim, and S. Lazarova-Molnar
On Device-level Majority von Neumann Multiplexing ***Invited***$_5$
Chapter 72 in J.R. Rabuñal et al. (Eds.): Encyclopedia of Artificial Intelligence
IGI Global, USA (Hershey, PA) and UK (London), 2009 (ISBN 9781599048499) 471–479
https://doi.org/10.4018/978-1-59904-849-9.ch072

Ch_5 V. Beiu, and W. Ibrahim: On Computing Nano-Architectures Using Unreliable Nano-Devices ***Invited***$_4$
Chapter 12 in S.E. Lyshevski (Ed.): Nano- and Molecular-Electronics Handbook
Taylor & Francis (UK/USA), May 2007 (ISBN 9780849385285) 1–49

Ch_4 V. Beiu: Entropy, Constructive Neural Learning, and VLSI Efficiency ***Invited***$_3$
In R. Andonie, and D. Grosu (Eds.): Neural Priorities in Data Transmission and EDA
Tempus SJEP 8180-94, "Transilvania" Univ. of Braşov, Braşov, Romania, 1998 38–74

Ch_3 V. Beiu: Constant Fan-in Discrete Neural Networks Are VLSI-Optimal
Chapter 12 in S.W. Ellacott, J.C. Mason, and I.J. Anderson (Eds.)
Mathematics of Neural Networks Models, Algorithms and Applications
Kluwer Academic, Boston, MA, USA, 1997 (ISBN 9781461377948) 89–94
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Ch_2 V. Beiu: Digital Integrated Circuit Implementations (of Neural Networks) ***Invited***$_2$
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Institute of Physics, New York, NY, USA, 1996 (ISBN 9780750303125) E1.4.1–34

Ch_1 V. Beiu: Optimal VLSI Implementations of Neural Networks ***Invited***$_1$
Chapter 18 in J.G. Taylor (Ed.): Neural Networks and Their Applications
John Wiley & Sons, Chichester, UK, 1996 (ISBN 9780471962823) 255–276

PATENTS 11

– V. Beiu: Procedure Enabling Statistical Meaningful Evaluation of Any Physical Feature or Figure-of-Merit of a Digital or Analog Circuit
UAEU Intellectual Property, July 16, 2014 & February 11, 2015 (Rouse Ref. U0018-00167) Submitted

P_{11} V. Beiu: Low-Power Differential Conductance-Based Logic Gate and Method of Operation Thereof
US 6,580,296, June 17, 2003 1–18
https://patents.google.com/patent/US6580296/

P_{10} V. Beiu: Microprocessor and a Digital Signal Processor Including Adder and Multiplier Circuits Employing Logic Gates Having Discrete and Weighted Inputs
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TW 481774, April 1, 2002 1–14
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P_3 V. Beiu: Logic Gate Having Reduced Power Dissipation and Method of Operation Thereof
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– V. Beiu: The Curse of Constant Failure Rates, Inputs and Averaging – A Comprehensive Review In planning
– V. Beiu: Brain-inspired Computing Revisited – Why Energy Consumption Is So Elusive In progress
– V. Beiu: The Trustworthy Wings of the Mysterious Butterflies In progress
– V. Beiu et al.: Revisiting Schmitt Trigger Tolerance to Variations In progress

– M. Nagy, S.R. Cowell, and V. Beiu: 3D Fibonacci Spirals Submitted
– M. Nagy, S.R. Cowell, and V. Beiu
Survey of Cubic Fibonacci Identities – When Cuboids Carry Weight Submitted
https://arxiv.org/abs/1902.05944
– L. Dauş, V. Beiu, S.R. Cowell, and P. Poulin: Brick-Wall Lattice Paths and Applications Submitted
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J_{38} V. Beiu: Brain Inspired Nano Architectures ***Invited***$_3$
Intl. J. Computers Communication & Control (IF ∼ 1.585, SJR ∼ 0.368) Accepted

J_{37} M. Tache, M. Balas, and V. Beiu
When Non-Gaussian Distributions Have to Be Considered
Theory and Applications of Mathematics & Computer Science Accepted

J_{36} V. Dragoi, S.R. Cowell, M. Nagy, and V. Beiu
A Preliminary Investigation of Matchstick Minimal Networks
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J_{35} V. Dragoi, and V. Beiu
Studying the Binary Erasure Polarization Subchannels Using Network Reliability
IEEE Comm. Lett., Oct. 2019 (IF ∼ 2.723, SJR ∼ 0.837) — Early Access
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J_{30} R.-M. Beiu, V. Beiu and V.-F. Duma
Fiber Optic Mechanical Deformation Sensors Employing Perpendicular Photonic Crystals
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– V. Beiu: Why Neural Energy/Power Is So Elusive — In progress
– M. Tache, and V. Beiu: On Hammock-based CMOS Inverters — In progress

2018 — 11

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C_{195} R.-M. Beiu, V.-F. Duma, and V. Beiu
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C_3 R. Munteanu, A. Aurelian, and V. Beiu: Ultra High Speed TTL Unit for a Graphic Workstation ***Best Paper Award***$_3$
Students Scientific Research Conference
Bucharest, Romania, May 17-18, 1980 731–735

1977 — **2**

C_2 V. Beiu: Field Effect Optoelectronic Equipments ***Best Paper Award***$_2$
Students' Scientific Research Conference
Bucharest, Romania, May 13-14, 1977 476–480

C_1 V. Beiu: Bistable Cholesteric Mixtures with Positive Dielectric Anisotropy ***Best Paper Award***$_1$
Students Scientific Research Conference
Bucharest, Romania, May 13-14, 1977 471–475

O_{51} R.-M. Beiu, M. M. Balas, V. E. Balas, and V. Beiu
Seeing is Believing
International Summit on Optics, Photonics and Laser Technologies OPTICS&LASERS'19
San Francisco, CA, USA, June 03-05, 2019

O_{50} M. Nagy, S. R. Cowell, and V. Beiu
Optimal Cubic Fibonacci Identities for 3D Packing
International Symposium Research and Education in Innovation Era ISREIE'19
Arad, Romania, May 23-25, 2019

O_{49} M. Tache, S. R. Cowell, and V. Beiu
Turning Sizing on Its Head and More
International Symposium Research and Education in Innovation Era ISREIE'19
Arad, Romania, May 23-25, 2019

O_{48} R.-M. Beiu, and V. Beiu
Sidestepping the Bounds of Diffraction
International Symposium Research and Education in Innovation Era ISREIE'19
Arad, Romania, May 23-25, 2019

O_{47} G. Cristescu, V. Dragoi, and V. Beiu
Cubic Spline Approximation of the Reliability Polynomials of Two Dual Hammock Networks
International Symposium Research and Education in Innovation Era ISREIE'19
Arad, Romania, May 23-25, 2019

O_{46} L. Hamad, A. Fahad, A. Saeed, F. Kharbash, and V. Beiu
On Reliability-Enhanced Quantum Cellular Automata (QCA) Designs
UAEU Annual Research & Innovation Conference ARIC'15
Al Ain, UAE, November 24-25, 2015

O_{45} L. Dauş, and V. Beiu: A Survey of Consecutive-*k*-out-of-*n* Systems Bounds
IEEE International Symposium on Multiple-Valued Logic ISMVL'14
International Workshop on Post-Binary ULSI Systems ULSIWS'14
Bremen, Germany, May 18-21, 2014

O_{44} M. Tache, V. Beiu, W. Ibrahim, F. Kharbash, and M. Alioto: Sizing for Static Noise Margins Revisited
European Workshop on CMOS Variability VARI'13/PATMOS'13
Karlsruhe, Germany, September 9-11, 2013

O_{43} V. Beiu, W. Ibrahim, A. Beg, and M. Tache: On Sizing Transistors for Threshold Voltage Variations
International Workshop on Design for Reliability DFR'12 (in conjunction with HiPEAC'12)
Paris, France, January 23-25, 2012
http://www.cs.ucy.ac.cy/carch/DFR2012/presentations/S2_3.pdf

O_{42} V. Beiu, and W. Ibrahim: NAND Multiplexing Down to Nuts and Bolts
International Conference on Ultimate Integration on Silicon ULIS'10
Glasgow, UK, March 17-19, 2010

O_{41} B.A.M. Madappuram, V. Beiu, and T.M. McGinnity
On Brain-inspired Hybrid Network Topologies for Future Nano-architectures ***Best Paper Award***$_1$
UAEU Annual Research Conference ARC-9, Al Ain, UAE, April 21-23, 2008

O_{40} S. Lazarova-Molnar, and V. Beiu
Mapping the Proxel-Based Method to Reliability Analysis of Nano-architectures
UAEU Annual Research Conference ARC-9, Al Ain, UAE, April 21-23, 2008

O_{39} R.M. Beiu, C.D. Stanescu, and V. Beiu
Nanostructured Fiber Optics as Highly Sensitive Mechanical Sensors ***Invited***$_7$
International Trends in NanoTechnology Conference TNT'07
San Sebastian, Spain, September 3-7, 2007

O_{38} W. Ibrahim, and V. Beiu
A Hybrid Monte-Carlo and Numerical Simulations Approach for Future Nano-circuits Reliability Calculation
International Trends in NanoTechnology Conference TNT'07
San Sebastian, Spain, September 3-7, 2007

O_{37} S. Lazarova-Molnar, V. Beiu, and W. Ibrahim: Proxels for Reliability Assessment of Future Nano-Circuits
International Trends in NanoTechnology Conference TNT'07
San Sebastian, Spain, September 3-7, 2007

O_{36} H. Amer, and V. Beiu: On Global Communications for Nano-Architectures – Brain versus Rent's Rule
International Trends in NanoTechnology Conference TNT'07
San Sebastian, Spain, September 3-7, 2007

O_{35} B.A.M. Madappuram, and V. Beiu
Using Standing Waves for Communications Might Work for Crossbar Architectures
International Trends in NanoTechnology Conference TNT'07
San Sebastian, Spain, September 3-7, 2007

O_{34} M.H. Sulieman, and V. Beiu: Investigating the Reliability of Single-Electron-Technology Gates and Circuits
UAEU Annual Research Conference ARC-8, Al Ain, UAE, April 23-25, 2007

O_{33} V. Beiu, J. Nyathi, and S. Aunet
Sub-Pico (Femto) Joule Switching: High-Speed Reliable CMOS Circuits Are Feasible
International Conference on Innovations in Information Technology IIT'05
Dubai, UAE, September 26-28, 2005
http://www.it-innovations.ae/iit005/proceedings/articles/E_5_IIT05_Beiu.pdf

O_{32} V. Beiu, S. Aunet, R. Rydberg III, A. Djupdal, and J. Nyathi
The Vanishing Majority Gate – Trading Power and Speed for Reliability
IEEE International Workshop on Design and Test of Defect-Tolerant
Nanoscale Architectures NanoArch'05, Palm Springs, CA, USA, May 1, 2005

O_{31} J. Nyathi, V. Beiu, and S. Aunet: Sub Femto Joule Switching – High Speed Reliable CMOS Circuits Are Feasible
ASILOMAR Conference on Signal, Systems and Computers
Pacific Groove, CA, USA, November 7-10, 2004

O_{30} J. Nyathi, V. Beiu, and S. Aunet
Femto Joule Switching – Review of Low Energy Design Styles for the Nano Era ***Invited***$_6$
International Symposium on Nano and Giga Challenges in Nanoelectronics NGCM'04
Krakow, Poland, September 13-17, 2004

O_{29} V. Beiu, U. Rückert, S. Roy, and J. Nyathi: On Nanoelectronic Architectural Challenges and Plausible Solutions
International Symposium on Nano and Giga Challenges in Nanoelectronics NGCM'04
Krakow, Poland, September 13-17, 2004

O_{28} V. Beiu, and A. Zawadzki: Why VLSI/Nano Library Design Should Use Kolmogorov's Superpositions
International Symposium on Nano and Giga Challenges in Nanoelectronics NGCM'04
Krakow, Poland, September 13-17, 2004

O_{27} V. Beiu: On Biological and Hardware Neural Networks ***Invited***$_5$
International Joint Meeting AMS-SMM, Denton, TX, USA, May 19-22, 1999

O_{26} V. Beiu, J. Frigo, and K.R. Moore: Why the Nervous Networks Are Reliable
International Symposium on Artificial Intelligence and Adaptive Systems CIMAF'99
Havana, Cuba, March 24-28, 1999

O_{25} V. Beiu, J. Frigo, and K.R. Moore: On the Reliability of Nervous Nets
International Conference on Computational Intelligence for Modeling,
Control and Automation CIMCA'99, Vienna, Austria, February 17-19, 1999

O_{24} S. Draghici, and V. Beiu: On Issues Related to VLSI Implementations of Neural Networks
International Conference on Cognitive and Neural Systems CNS'98
Boston, MA, USA, May 27-30, 1998

O_{23} V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins
Digital Implementation of Neural Networks Using Threshold Gates
International Conference Romania and Romanians in Contemporary Science
Sinaia, Romania, May 24-27, 1994
http://citeseerx.ist.psu.edu/viewdoc/citations;jsessionid=E6CF9AE07D31AEDC41844D7E839B9EAB?doi=10.1.1.30.8504

O_{22} D.O. Creteanu, and V. Beiu: Systolic Pattern Recognition System
International Conference on Fuzzy Systems and Artificial Intelligence IFSAI'92
Iaşi, Romania, October 28-31, 1992

O_{21} V. Beiu, D.C. Ioan, M. Dumbrava, and O. Robciuc
Physical Fields Determination Using Continuous Boltzmann Machines ***Invited***$_4$
Symposium on Parallel Computing, Bucharest, Romania, December 10-11, 1991

O_{20} V. Beiu: Motion Detection with Neural Networks
International Conference on Industrial and Applied Mathematics ICIAM'91
Washington DC, USA, July 8-12, 1991

O_{19} V. Beiu: Neural Network Solutions for Motion Detection
International Symposium on Applied Informatics, Innsbruck, Austria, February 18-21, 1991

O_{18} A. Florea, V. Beiu, and S. Georgescu: Expert System Development with a Neural Network Simulator
International Conference on AI and Control Systems for Robots AICSR'89
Strbskoe Pleso, Czechoslovakia, November 6-10, 1989

O_{17} V. Beiu: From Systolic Arrays to Neural Networks ***Invited***$_3$
International Symposium on Informatics INFO-IASI'89
Iaşi, Romania, October 19-21, 1989

O_{16} M. Constantinescu, and V. Beiu: Theoretical Aspects of Parallel Algorithms for Histogram Modification
International Conference on Computer Systems MICROSYSTEM'89
Carlsbad (Karlovy Vary), Czechoslovakia, September 18-21, 1989

O_{15} V. Beiu, and S. Georgescu: Neural Network Models of Vision
IAPR Workshop on Computer Vision, Tokyo, Japan, October 12-14, 1988

O_{14} A. Florea, and V. Beiu: Expert Decisions Using Neural Models
Conference on Electronics, Telecommunication, Control and Computers CNETAC'88
Bucharest, Romania, December 7-9, 1988

O_{13} V. Beiu: Hierarchical Memory Enhanced with List Processing Facilities
International Conference on Computer Systems MICROSYSTEM'88
Bratislava, Czechoslovakia, August 30 - September 1, 1988

O_{12} V. Beiu: Parallel Line-Drawing Algorithms
International Conference on Computer Systems MICROSYSTEM'88
Bratislava, Czechoslovakia, August 30 - September 1, 1988

O_{11} V. Beiu. M. Ionescu, E. Paşol, and L. Zuzu: VLSI Implementation of a Statistical Multiplexer
International Symposium Mini and Microcomputers ISMM-MIMI'87
Lugano, Switzerland, June 29 - July 2, 1987

O_{10} V. Beiu, M. Ionescu, E. Paşol, and L. Zuzu: Adaptive Multiplexing Algorithm and Its Possible VLSI Implementation
Mediterranean Electrotechnical Conference MELECON'87, Rome, Italy, March 24-26, 1987

O_9 V. Beiu: Smart Image Memory for Parallel Line Generation
Conference on Electronics, Telecommunication, Control and Computers CNETAC'86
Bucharest, Romania, December 4-6, 1986

O_8 F. Moraru, C. Ispas, S. Constantin, A. Niculescu, and V. Beiu: Automat Conical Ball Bearing Sorting System
National Conference on Automatic Measurement Systems Using Computer Techniques
Bucharest, Romania, May 22-24, 1986

O_7 V. Beiu: Parallel Adder with Regular Structure
Conference on Electronics, Telecommunication, Control and Computers CNETAC'85
Bucharest, Romania, November 21-23, 1985

O_6 V. Beiu: Self-Testable and Self-Repairable Units – A Must for VLSI Structures
Conference on Electronics, Telecommunication, Control and Computers CNETAC'84
Bucharest, Romania, November 22-24, 1984

O_5 V. Beiu: High Reliability Memory Organization
Conference on Electronics, Telecommunication, Control and Computers CNETAC'83
Bucharest, Romania, November 17-18, 1983

O_4 V. Beiu: Using Microprocessors in Audio Systems
Conference on Electronics, Telecommunication, Control and Computers CNETAC'82
Bucharest, Romania, November 17-19, 1982

O_3 V. Beiu: Memory Structure with Simultaneous Read and Write Capabilities ***Invited***$_2$
Military Academy of Sciences, Bucharest, Romania, November, 1982

O_2 V. Beiu: Method for Storing Digital Information on a Video Recorder
Conference on Electronics, Telecommunication, Control and Computers CNETAC'81
Bucharest, Romania, November, 1981

O_1 V. Beiu: Reliability Enhanced Memory Architecture with Gracefully Degrading Performances ***Invited***$_1$
Jubilee: Ten Years from the Foundation of the National College of Informatics
Bucharest, Romania, May, 1981

TECHNICAL REPORTS 67

Remark: 25 have appeared only as technical reports, while 42 have also been published (conferences/journals)

TR_{67} V. Beiu: WTEC-NANO2 (21 pages)
International Study of the Long-term Impacts and Future Opportunities for
Nanoscale Science and Engineering, September 2010

TR_{66} V. Beiu, H.E. Makaruk, D. Morgan, and L. Popa-Simil
ARGOS Advanced RTR (Real Time Radiography) Graphical Object Selection
Los Alamos Unrestricted Report LA-UR-03-2477, April 2003

TR_{65} V. Beiu, H.E. Makaruk, D. Morgan, and L. Popa-Simil: ARGOS – The Problem
Los Alamos Unrestricted Report LA-UR-03-2474, April 2003

TR_{64} V. Beiu: On Automatic Synthesis of Analog/Digital Circuits
Los Alamos Unrestricted Report LA-UR-98-3463, 1998

TR_{63} V. Beiu: Larger Bases and Mixed Analog/Digital Neural Networks
Los Alamos Unrestricted Report LA-UR-98-3462, 1998

TR_{62} V. Beiu, J. Frigo, and K.R. Moore: On the Reliability of Nervous Nets
Los Alamos Unrestricted Report LA-UR-98-3461, 1998

TR_{61} V. Beiu: Neural Inspired Parallel Computations Require Analog Processors
Los Alamos Unrestricted Report LA-UR-98-3325, 1998

TR_{60} V. Beiu, and S. Draghici: Designing Constructive Neural Learning Algorithms Based on Information Entropy Bounds
Los Alamos Unrestricted Report LA-UR-98-3168, 1998

TR_{59} V. Beiu: On Kolmogorov's Superposition and Boolean Functions
Los Alamos Unrestricted Report LA-UR-98-2883, 1998

TR_{58} V. Beiu: 2D Neural Hardware vs 3D Biological Ones
Los Alamos Unrestricted Report LA-UR-98-2504, 1998

TR_{57} V. Beiu, S. Draghici, and T. De Pauw: A Constructive Approach to Calculating Lower Entropy Bounds
Los Alamos Unrestricted Report LA-UR-98-2333, 1998

TR_{56} V. Beiu: Implementing Size-Optimal Discrete Neural Networks Requires Analog Circuitry
Los Alamos Unrestricted Report LA-UR-98-1702, 1998

TR_{55} V. Beiu, and K.R. Moore: On Analog Implementation of Discrete Neural Networks
Los Alamos Unrestricted Report LA-UR-98-1609, 1998

TR_{54} V. Beiu: How to Build VLSI-Efficient Neural Chips
Los Alamos Unrestricted Report LA-UR-97-4460, 1997

TR_{53} V. Beiu: Implementing Size-Optimal Discrete Neural Networks Requires Analog Circuitry
Los Alamos Unrestricted Report LA-UR-97-4432, 1997

TR_{52} V. Beiu, and H.E. Makaruk: On Deeper Nets for Classification Problems
Los Alamos Unrestricted Report LA-UR-97-4413, 1997

TR_{51} V. Beiu, and H.E. Makaruk: Deeper and Sparser Nets Are Optimal
Los Alamos Unrestricted Report LA-UR-97-4359, 1997

TR_{50} V. Beiu, S. Draghici, and H.E. Makaruk: On Limited Fan-In Optimal Neural Networks
Los Alamos Unrestricted Report LA-UR-97-4314, 1997

TR_{49} V. Beiu, and H.E. Makaruk
Constructive Entropy Bounds Based on n-Dimensional Complexes
Los Alamos Unrestricted Report LA-UR-97-4251, 1997

TR_{48} V. Beiu, and H.E. Makaruk: Small Fan-In Is Beautiful
Los Alamos Unrestricted Report LA-UR-97-3493, 1997

TR_{47} V. Beiu: On the Circuit and VLSI Complexity of Threshold Gate COMPARISON
Los Alamos Unrestricted Report LA-UR-97-3353, 1997

TR_{46} V. Beiu, and S. Draghici: On Sparsely Connected Optimal Neural Networks
Los Alamos Unrestricted Report LA-UR-97-2970, 1997

TR_{45} V. Beiu, and H.E. Makaruk
Computing Volumes of n-Dimensional Complexes
Los Alamos Unrestricted Report LA-UR-97-2873, 1997

TR_{44} V. Beiu: Entropy, Constructive Neural Learning, and VLSI Efficiency
Los Alamos Unrestricted Report LA-UR-97-2843, 1997

TR_{43} V. Beiu: The Next Generation of Neural Networks Chips
Los Alamos Unrestricted Report LA-UR-97-1917, 1997

TR_{42} V. Beiu: When Reduced Connectivity Neural Networks Are Complexity Optimal?
Los Alamos Unrestricted Report LA-UR-97-1916, 1997

TR_{41} V. Beiu: Digital Integrated Circuit Implementations (of Neural Networks)
Los Alamos Unrestricted Report LA-UR-97-1900, 1997

TR_{40} V. Beiu: Enhanced Lower Entropy Bounds with Application to Constructive Learning
Los Alamos Unrestricted Report LA-UR-97-1877, 1997

TR_{39} S. Draghici, V. Beiu, and I.K. Sethi: A VLSI Optimal Constructive Algorithm for Classification Problems
Los Alamos Unrestricted Report LA-UR-97-1609, 1997

TR_{38} V. Beiu, and S. Draghici: On Sparsely Connected Optimal Neural Networks
Los Alamos Unrestricted Report LA-UR-97-1567, 1997

TR_{37} V. Beiu: When Constants Are Important
Los Alamos Unrestricted Report LA-UR-97-1262, 1997

TR_{36} V. Beiu, S. Draghici, and T. De Pauw: A Constructive Approach to Calculating Lower Entropy Bounds
Los Alamos Unrestricted Report LA-UR-97-884, 1997

TR_{35} V. Beiu: Optimization of Circuits Using a Constructive Neural Network Learning Algorithm
Los Alamos Unrestricted Report LA-UR-97-851, 1997

TR_{34} V. Beiu: Enhanced Lower Entropy Bounds with Application to Constructive Learning
Los Alamos Unrestricted Report LA-UR-97-516, 1997

TR_{33} V. Beiu: Reduced Complexity Constructive Learning Algorithm
Los Alamos Unrestricted Report LA-UR-97-515, 1997

TR_{32} S. Draghici, and V. Beiu: Entropy Based Comparison of Neural Networks for Classification
Los Alamos Unrestricted Report LA-UR-97-483, 1997

TR_{31} V. Beiu, and S. Draghici: Limited Weights Neural Networks: Very Tight Entropy Based Bounds
Los Alamos Unrestricted Report LA-UR-97-294, 1997

TR_{30} V. Beiu: When Constants Are Important
Los Alamos Unrestricted Report LA-UR-97-226, 1997

TR_{29} V. Beiu: Constant Fan-In Discrete Neural Networks Are VLSI-Optimal
Los Alamos Unrestricted Report LA-UR-97-61, 1997

TR_{28} V. Beiu, and T. De Pauw: Tight Bounds on the Size of Neural Networks for Classification Problems
Los Alamos Unrestricted Report LA-UR-97-60, 1997

TR_{27} V. Beiu: Optimization of Circuits Using a Constructive Neural Network Learning Algorithm
Los Alamos Unrestricted Report LA-UR-97-59, 1997

TR_{26} V. Beiu: On the Circuit and VLSI Complexity of Threshold Gate COMPARISON
Los Alamos Unrestricted Report LA-UR-96-3591, 1996

TR_{25} V. Beiu: New VLSI Complexity Results for Threshold Gate COMPARISON
Los Alamos Unrestricted Report LA-UR-96-3576, 1996

TR_{24} J.C. Lemm, V. Beiu, and J.G. Taylor
Density Estimation as a Preprocessing Step for Constructive Algorithms
Munster University Technical Report MS-TPI-95-10, 1995

TR_{23} V. Beiu, D.C. Ioan, M. Dumbrava, and O. Robciuc
Physical Fields Determination Using Continuous Boltzmann Machines
Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, December 1991

TR_{22} V. Beiu: Motion Detection with Neural Networks
Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, September 1991

TR_{21} V. Beiu: Neural Network Solutions for Motion Detection
Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, March 1991

TR_{20} V. Beiu: Neural Network Priority Queue
Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, October 1990

TR_{19} A. Florea, V. Beiu, and S. Georgescu: Expert System Development with a Neural Network Simulator
Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, December 1989

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TR_{17} M. Constantinescu, and V. Beiu: Theoretical Aspects of Parallel Algorithms for Histogram Modification
Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, October 1989

TR_{16} V. Beiu, and A. Florea: Basic Structure of a Program Used to Simulate Processor Networks
Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, December 1988

TR_{15} A. Florea, and V. Beiu: Expert Decisions Using Neural Models
Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, December 1988

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Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, October 1988

TR_{13} V. Beiu: Parallel Line-Drawing Algorithms
Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, October 1988

TR_{12} V. Ivanov, and V. Beiu: Heuristic Simulation of Circuits Using PROLOG
Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, February 1988

TR_{11} V. Beiu, M. Ionescu, E. Paşol, and L. Zuzu: VLSI Implementation of a Statistical Multiplexer
Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, September 1987

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Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, April 1987

TR_{9} V. Beiu: Smart Image Memory for Parallel Line Generation
Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, December 1986

TR_{8} F. Moraru, C. Ispas, S. Constantin, A. Niculescu, and V. Beiu: Automat Conical Ball Bearing Sorting System
Technical Report, Department of Mechanics, University "Politehnica" of Bucharest, Romania, June 1986

TR_{7} V. Beiu: Parallel Adder with Regular Structure
Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, December 1985

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Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, December 1983

TR_{4} V. Beiu: Memory Structure with Simultaneous Read and Write Capabilities
Technical Report, Military Academy of Sciences, Bucharest, Romania, November 1982

TR_{3} V. Beiu: Using Microprocessors in Audio Systems
Technical Report, Research Institute for Computer Technique, Bucharest, Romania, December 1982

TR_{2} V. Beiu: Method for Recording Digital Information on a Video Recorder
Technical Report, Research Institute for Computer Technique, Bucharest, Romania, December 1981

TR_{1} V. Beiu: Reliability Enhanced Memory with Gracefully Degrading Performances
Technical Report, Research Institute for Computer Technique, Bucharest, Romania, July 1981