

	PUBLICATE	ACCEPTATE
CARTI	2	3
CAPITOLE	8 (7 INVITATE)	5
BREVETE	11	
REVISTE	35 (2 INVITATE)	3 (1 INVITATA)
CONFERINTE	207 (26 INVITATE)	
TOTAL	274 (36 INVITATE, 7 BEST PAPER AWARDS)	
ALTE CONFERINTE RAPOARTE TEHNICE	51 (7 INVITATE, 1 BEST PAPER AWARD)	67

CARTI 2

- V. Beiu, and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures
Book in progress (contract signed with World Scientific)
- V. Beiu: VLSI Complexity of Discrete Neural Networks
Book in progress (contract signed with Taylor & Francis)
- V. Beiu, R. Andonie, and R. Dogaru: Fundamental Problems of Neural Networks
Book in progress (contract signed with Technical Printing House)

- B₂ V. Beiu, and S. Harous (Eds.): Innovations
IEEE Press, November 2014 (ISBN 9781479972128) 1–132
<https://ieeexplore.ieee.org/document/6985768/>
- B₁ A. Schmid, S. Goel, W. Wang, V. Beiu, and S. Carrara (Eds.): Nano-Net
Springer, LNICS, October 2009 (ISBN 9783642024276) 1–286
<https://doi.org/10.1007/978-3-642-04850-0>
- … V. Beiu: Neural Networks Using Threshold Gates
A Complexity Analysis of Their Area- and Time-Efficient VLSI Implementations
PhD dissertation, Katholieke Universiteit Leuven, Leuven, Belgium
U.D.C. 621.3.04977: 681.3*C13 (x-27-151779-3), May 1994 1–222

CAPITOLE (7 INVITATE) 8

- V. Beiu, and W. Ibrahim: On Enabling Redundant Designs for Nano Computations
In V. Beiu, and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures
- V. Beiu, J.M. Quintana, and M.J. Avedillo
Threshold Logic Design and Implementations: From the Early Days into the Nanoera
In V. Beiu, and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures
- M.H. Sulieman, and V. Beiu
From Single Electron Technology (SET) Full Adders to Optimal Practical SET Adders
In V. Beiu, and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures
- V. Beiu, and U. Rückert: Roadmap for Nano Architectures
In V. Beiu, and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures
- J. Nyathi, and V. Beiu: Advanced Techniques for Reducing Power Consumption
In V. Beiu, and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures

Ch ₈	V. Beiu, L. Zhang, A. Beg, W. Ibrahim, and M. Tache: Axon-Inspired Communication Systems Chapter 15 in J.E. Morris and K. Iniewski (Eds.): Nanoelectronic Device Applications Handbook, CRC/Taylor & Francis (UK/USA), 2013 (ISBN 9781466565234)	<i>Invited₇</i>	193–208
Ch ₇	A. Beg, M.H. Sulieman, V. Beiu, and W. Ibrahim: Low-Power Reliable Nano Adders Chapter 6 in J.E. Morris and K. Iniewski (Eds.): Nanoelectronic Device Applications Handbook, CRC/Taylor & Francis (UK/USA), 2013 (ISBN 9781466565234)	<i>Invited₆</i>	67–75
Ch ₆	V. Beiu, W. Ibrahim, and S. Lazarova-Molnar On Device-level Majority von Neumann Multiplexing Chapter 72 in J.R. Rabuñal et al. (Eds.): Encyclopedia of Artificial Intelligence IGI Global, USA (Hershey, PA) and UK (London), 2009 (ISBN 9781599048499) https://doi.org/10.4018/978-1-59904-849-9.ch072	<i>Invited₅</i>	471–479
Ch ₅	V. Beiu, and W. Ibrahim: On Computing Nano-Architectures Using Unreliable Nano-Devices Chapter 12 in S.E. Lyshevski (Ed.): Nano- and Molecular-Electronics Handbook Taylor & Francis (UK/USA), May 2007 (ISBN 9780849385285)	<i>Invited₄</i>	1–49
Ch ₄	V. Beiu: Entropy, Constructive Neural Learning, and VLSI Efficiency In R. Andonie, and D. Grosu (Eds.): Neural Priorities in Data Transmission and EDA Tempus SJEPE 8180-94, "Transilvania" Univ. of Braşov, Braşov, Romania, 1998	<i>Invited₃</i>	38–74
Ch ₃	V. Beiu: Constant Fan-in Discrete Neural Networks Are VLSI-Optimal Chapter 12 in S.W. Ellacott, J.C. Mason, and I.J. Anderson (Eds.) Mathematics of Neural Networks Models, Algorithms and Applications Kluwer Academic, Boston, MA, USA, 1997 (ISBN 9781461377948) https://doi.org/10.1007/978-1-4615-6099-9_12		89–94
Ch ₂	V. Beiu: Digital Integrated Circuit Implementations (of Neural Networks) Chapter E1.4 in E. Fiesler, and R. Beale (Eds.): Handbook of Neural Computations Institute of Physics, New York, NY, USA, 1996 (ISBN 9780750303125)	<i>Invited₂</i>	E1.4.1–34
Ch ₁	V. Beiu: Optimal VLSI Implementations of Neural Networks Chapter 18 in J.G. Taylor (Ed.): Neural Networks and Their Applications John Wiley & Sons, Chichester, UK, 1996 (ISBN 9780471962823)	<i>Invited₁</i>	255–276

BREVETE

11

–	V. Beiu: Procedure Enabling Statistical Meaningful Evaluation of Any Physical Feature or Figure-of-Merit of a Digital or Analog Circuit UAEU Intellectual Property, July 16, 2014 & February 11, 2015 (Rouse Ref. U0018-00167)	Submitted
P ₁₁	V. Beiu: Low-Power Differential Conductance-Based Logic Gate and Method of Operation Thereof US 6,580,296, June 17, 2003 https://patents.google.com/patent/US6580296/	1–18
P ₁₀	V. Beiu: Microprocessor and a Digital Signal Processor Including Adder and Multiplier Circuits Employing Logic Gates Having Discrete and Weighted Inputs US 6,516,331, February 4, 2003 https://patents.google.com/patent/US6516331/	1–14
P ₉	V. Beiu: Adder Circuits Employing Logic Gates Having Discrete Weighted Inputs and a Method of Operation Therewith US 6,502,120, December 31, 2002 https://patents.google.com/patent/US6502120/	1–13

P ₈	V. Beiu: Adder Having Reduced Number of Internal Layers and Method of Operation Thereof US 6,438,572, August 20, 2002 [Also as WO/2001/023992 and AU40251/01] https://patents.google.com/patent/US6438572/	1–11
P ₇	V. Beiu: Noise Tolerant Conductance-Based Logic Gate and Methods of Operation and Manufacturing Thereof US 6,430,585, August 6, 2002 [Also as WO/2001/024367 and AU76009/00] https://patents.google.com/patent/US6430585/	1–16
P ₆	V. Beiu: Adder Having Reduced Number of Internal Layers and Method of Operation Thereof TW 493139, July 1, 2002 https://twpat1.tipo.gov.tw/tipotwoc/tipotwekm?!IFR_493139	1–15
P ₅	V. Beiu: Noise Tolerant Conductance-Based Logic Gate and Methods of Operation and Manufacturing Thereof TW 483249, April 11, 2002 https://twpat1.tipo.gov.tw/tipotwoc/tipotwekm?!IFR_483249	1–13
P ₄	V. Beiu: Adder and Multiplier Circuits Employing Logic Gates Having Discrete, Weighted Inputs and Methods of Performing Combinatorial Operations Therewith TW 481774, April 1, 2002 https://twpat1.tipo.gov.tw/tipotwoc/tipotwekm?!IFR_481774	1–14
P ₃	V. Beiu: Logic Gate Having Reduced Power Dissipation and Method of Operation Thereof US 6,259,275, July 10, 2001 https://patents.google.com/patent/US6259275/	1–19
P ₂	V. Beiu: Adder and Multiplier Circuits Employing Logic Gates Having Discrete, Weighted Inputs and Methods of Performing Combinatorial Operations Therewith US 6,205,458, March 20, 2001 [Also as WO/2000/017802 and AU58155/99] https://patents.google.com/patent/US6205458/	1–14
P ₁	V. Beiu: LSI Unit for Mutual Exclusion RO 84763, April 26, 1984	1–12

REVISTE (3 INVITATE)

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–	V. Beiu: The Curse of Constant Failure Rates, Inputs and Averaging – A Comprehensive Review	In planning
–	V. Beiu: Brain-inspired Computing Revisited – Why Energy Consumption Is So Elusive	In progress
–	V. Beiu: The Trustworthy Wings of the Mysterious Butterflies	In progress
–	V. Beiu et al.: Revisiting Schmitt Trigger Tolerance to Variations	In progress
–	M. Nagy, S.R. Cowell, and V. Beiu: 3D Fibonacci Spirals	Submitted
–	M. Nagy, S.R. Cowell, and V. Beiu Survey of Cubic Fibonacci Identities – When Cuboids Carry Weight https://arxiv.org/abs/1902.05944	Submitted
–	L. Daus, V. Beiu, S.R. Cowell, and P. Poulin: Brick-Wall Lattice Paths and Applications https://arxiv.org/abs/1804.05277	Submitted
J ₃₈	V. Beiu: Brain Inspired Nano Architectures Intl. J. Computers Communication & Control (IF ~ 1.585, SJR ~ 0.368)	<i>Invited</i> ₃ Accepted
J ₃₇	M. Tache, M. Balas, and V. Beiu When Non-Gaussian Distributions Have to Be Considered Theory and Applications of Mathematics & Computer Science	Accepted

- J₃₆ V. Dragoi, S.R. Cowell, M. Nagy, and V. Beiu
A Preliminary Investigation of Matchstick Minimal Networks
Theory and Applications of Mathematics & Computer Science Accepted
- J₃₅ V. Dragoi, and V. Beiu
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Compared with Hammocks?
Intl. J. Comp. Comm. & Ctrl., vol. 13, no. 5, Oct. 2018 (IF = 1.585, SJR ~ 0.368) 772–791
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- J₁ E. Oltean, and V. Beiu: Numerical Aspects in the Implementation of Self-Tuning Algorithms
UPB Scientific Bulletin, Control & Computers, vol. AC-48, 1986 (SJR later) 79–92

- V. Beiu: Why the Brain Can and Silicon Can't – The Energy Conundrum In progress
- V. Beiu: Why Neural Energy/Power Is So Elusive In progress
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2018

11

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- C₂₀₆ V. Beiu, S.R. Cowell, and V. Dragoi
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 International Workshop on Soft Computing Applications SOFA'18
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- C₂₀₃ V. Dragoi, S.R. Cowell, M. Nagy, and V. Beiu : Matchstick Minimal Circuits
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- C₂₀₂ R.-M. Beiu, V.-F. Duma, and V. Beiu
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 Baile Felix/Oradea, Romania, May 08-12, 2018 136–141
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- C₂₀₁ N.-C. Rohatinovici, S.R. Cowell, L. Daus, P. Poulin, V. Dragoi, V.E. Balas, and V. Beiu
 On Algorithms for Evaluating the Reliability of Large Hammock Networks
 IEEE International Conference on Computers Communications and Control ICCCC'18
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- C₂₀₀ V. Dragoi, S.R. Cowell, S. Hoara, P. Gaspar, and V. Beiu
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- C₁₉₈ M. Nagy, S.R. Cowell, and V. Beiu
Are 3D Fibonacci Spirals for Real ? — From Science to Arts and Back to Science
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Baile Felix/Oradea, Romania, May 08-12, 2018 91–96
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- C₁₉₇ R.-M. Beiu, V. Beiu, and V.-F. Duma: Ultra-small Mechanical Deformation Sensor
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2017

6

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Pittsburgh, USA, July 25-28, 2017 185–188
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- C₁₉₅ R.-M. Beiu, V.-F. Duma, and V. Beiu
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SPIE-SRLS International Conference for Lasers in Medicine ICLM'17
Timisoara, Romania, July 13-15, 2017 108310I(1–4)
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67

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