

OVERVIEW	PUBLISHED	ACCEPTED
BOOKS	2	3
CHAPTERS	8 (7 INVITED)	5
PATENTS	11	
JOURNALS	37 (2 INVITED)	5 (1 INVITED)
CONFERENCES	219 (28 INVITED)	
<b>TOTAL</b>	<b>290 (38 INVITED, 8 BEST PAPER AWARDS)</b>	
OTHER CONFERENCES	51 ( 7 INVITED, 1 BEST PAPER AWARD)	
TECHNICAL REPORTS	71	

## BOOKS 2

- V. Beiu, and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures  
Book in progress (contract signed with World Scientific)
- V. Beiu: VLSI Complexity of Discrete Neural Networks  
Book in progress (contract signed with Taylor & Francis)
- V. Beiu, R. Andonie, and R. Dogaru: Fundamental Problems of Neural Networks  
Book in progress (contract signed with Technical Printing House)
- B<sub>2</sub> V. Beiu, and S. Harous (Eds.): Innovations  
IEEE Press, November 2014 (ISBN 9781479972128) 1–132  
<https://doi.org/10.1109/INNOVATIONS.2014.6985768>
- B<sub>1</sub> A. Schmid, S. Goel, W. Wang, V. Beiu, and S. Carrara (Eds.): Nano-Net  
Springer, LNICS, October 2009 (ISBN 9783642024276) 1–286  
<https://doi.org/10.1007/978-3-642-04850-0>
- … V. Beiu: Neural Networks Using Threshold Gates  
A Complexity Analysis of Their Area- and Time-Efficient VLSI Implementations  
*PhD dissertation (summa cum laude)*, Katholieke Universiteit Leuven, Leuven, Belgium  
U.D.C. 621.3.04977: 681.3\*C13 (x-27-151779-3), May 1994 1–222

## CHAPTERS (7 INVITED) 8

- V. Beiu, and W. Ibrahim: On Enabling Redundant Designs for Nano Computations  
In V. Beiu, and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures
- V. Beiu, J.M. Quintana, and M.J. Avedillo  
Threshold Logic Design and Implementations: From the Early Days into the Nanoera  
In V. Beiu, and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures
- M.H. Sulieman, and V. Beiu  
From Single Electron Technology (SET) Full Adders to Optimal Practical SET Adders  
In V. Beiu, and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures
- V. Beiu, and U. Rückert: Roadmap for Nano Architectures  
In V. Beiu, and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures
- J. Nyathi, and V. Beiu: Advanced Techniques for Reducing Power Consumption  
In V. Beiu, and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures
- Ch<sub>8</sub> V. Beiu, L. Zhang, A. Beg, W. Ibrahim, and M. Tache: Axon-Inspired Communication Systems *Invited*,  
Chapter 15 in J.E. Morris and K. Iniewski (Eds.): Nanoelectronic Device Applications  
Handbook, CRC/Taylor & Francis (UK/USA), 2013 (ISBN 9781466565234) 193–208

Ch <sub>7</sub>	A. Beg, M.H. Sulieman, V. Beiu, and W. Ibrahim: Low-Power Reliable Nano Adders Chapter 6 in J.E. Morris and K. Iniewski (Eds.): Nanoelectronic Device Applications Handbook, CRC/Taylor & Francis (UK/USA), 2013 (ISBN 9781466565234)	<i>Invited<sub>6</sub></i>	67–75
Ch <sub>6</sub>	V. Beiu, W. Ibrahim, and S. Lazarova-Molnar On Device-level Majority von Neumann Multiplexing Chapter 72 in J.R. Rabuñal et al. (Eds.): Encyclopedia of Artificial Intelligence IGI Global, USA (Hershey, PA) and UK (London), 2009 (ISBN 9781599048499) <a href="https://doi.org/10.4018/978-1-59904-849-9.ch072">https://doi.org/10.4018/978-1-59904-849-9.ch072</a>	<i>Invited<sub>5</sub></i>	471–479
Ch <sub>5</sub>	V. Beiu, and W. Ibrahim: On Computing Nano-Architectures Using Unreliable Nano-Devices Chapter 12 in S.E. Lyshevski (Ed.): Nano- and Molecular-Electronics Handbook Taylor & Francis (UK/USA), May 2007 (ISBN 9780849385285)	<i>Invited<sub>4</sub></i>	1–49
Ch <sub>4</sub>	V. Beiu: Entropy, Constructive Neural Learning, and VLSI Efficiency In R. Andonie, and D. Grosu (Eds.): Neural Priorities in Data Transmission and EDA Tempus SJEP 8180-94, “Transilvania” Univ. of Braşov, Braşov, Romania, 1998	<i>Invited<sub>3</sub></i>	38–74
Ch <sub>3</sub>	V. Beiu: Constant Fan-in Discrete Neural Networks Are VLSI-Optimal Chapter 12 in S.W. Ellacott, J.C. Mason, and I.J. Anderson (Eds.) Mathematics of Neural Networks Models, Algorithms and Applications Kluwer Academic, Boston, MA, USA, 1997 (ISBN 9781461377948) <a href="https://doi.org/10.1007/978-1-4615-6099-9_12">https://doi.org/10.1007/978-1-4615-6099-9_12</a>		89–94
Ch <sub>2</sub>	V. Beiu: Digital Integrated Circuit Implementations (of Neural Networks) Chapter E1.4 in E. Fiesler, and R. Beale (Eds.): Handbook of Neural Computations Institute of Physics, New York, NY, USA, 1996 (ISBN 9780750303125)	<i>Invited<sub>2</sub></i>	E1.4.1–34
Ch <sub>1</sub>	V. Beiu: Optimal VLSI Implementations of Neural Networks Chapter 18 in J.G. Taylor (Ed.): Neural Networks and Their Applications John Wiley & Sons, Chichester, UK, 1996 (ISBN 9780471962823)	<i>Invited<sub>1</sub></i>	255–276

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P <sub>10</sub>	V. Beiu: Microprocessor and a Digital Signal Processor Including Adder and Multiplier Circuits Employing Logic Gates Having Discrete and Weighted Inputs US 6,516,331, February 4, 2003 <a href="https://patents.google.com/patent/US6516331/">https://patents.google.com/patent/US6516331/</a>		1–14
P <sub>9</sub>	V. Beiu: Adder Circuits Employing Logic Gates Having Discrete Weighted Inputs and a Method of Operation Therewith US 6,502,120, December 31, 2002 <a href="https://patents.google.com/patent/US6502120/">https://patents.google.com/patent/US6502120/</a>		1–13
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P <sub>4</sub>	V. Beiu: Adder and Multiplier Circuits Employing Logic Gates Having Discrete, Weighted Inputs and Methods of Performing Combinatorial Operations Therewith TW 481774, April 1, 2002 <a href="https://twpat1.tipo.gov.tw/tipotwoc/tipotwekm?!!FR_481774">https://twpat1.tipo.gov.tw/tipotwoc/tipotwekm?!!FR_481774</a>	1–14
P <sub>3</sub>	V. Beiu: Logic Gate Having Reduced Power Dissipation and Method of Operation Thereof US 6,259,275, July 10, 2001 <a href="https://patents.google.com/patent/US6259275/">https://patents.google.com/patent/US6259275/</a>	1–19
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...	V. Beiu et al.: The Curse of Constant Failure Rates, Inputs and Averaging – A Comprehensive Review	In planning
...	V. Beiu et al.: Brain-inspired Computing Revisited – Why Energy Consumption Is So Elusive	In progress
...	V. Beiu et al.: The Trustworthy Wings of the Mysterious Butterflies	In progress
...	V. Beiu et al.: Revisiting Schmitt Trigger Tolerance to Variations	In progress
J <sub>42</sub>	S.R. Cowell, S. Hoara, and V. Beiu Approximating Hammocks' Reliability with Beta Distributions Intl. J. Computers Communication & Control (IF ~ 2.293, SJR ~ 0.422)	Accepted
J <sub>41</sub>	M. Nagy, S.R. Cowell, and V. Beiu: Survey of Cubic Fibonacci Identities Intl. J. Computers Communication & Control (IF ~ 2.293, SJR ~ 0.422)	Accepted
J <sub>40</sub>	V. Beiu: Brain Inspired Nano Architectures Intl. J. Computers Communication & Control (IF ~ 2.293, SJR ~ 0.422)	<i>Invited</i> <sub>3</sub> Accepted
J <sub>39</sub>	M. Tache and V. Beiu When Non-Gaussian Distributions Have to Be Considered Theory and Applications of Mathematics & Computer Science	Accepted
J <sub>38</sub>	V. Dragoi, S.R. Cowell, M. Nagy, and V. Beiu A Preliminary Investigation of Matchstick Minimal Networks Theory and Applications of Mathematics & Computer Science	Accepted

- J<sub>37</sub> V. Dragoi, S.R. Cowell, and V. Beiu  
Four Input Sorter Good, Larger Ones Not So Good  
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Fast Reliability Ranking of Matchstick Minimal Networks  
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- V. Beiu: Why the Brain Can and Silicon Can't – The Energy Conundrum In progress
- V. Beiu: Why Neural Energy/Power Is So Elusive In progress
- M. Tache, and V. Beiu: On Hammock-based CMOS Inverters In progress
- M. Tache, V. Dragoi, L. Daus, and V. Beiu:  
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2021

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- C<sub>219</sub> V. Beiu: The Unfolding Road from Dust to Trust *Invited*<sub>28</sub>  
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2020

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- C<sub>218</sub> V. Beiu, V. Dragoi, and R.-M. Beiu  
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 computation will depend on large numbers of nanoscale devices and networks with varying degrees of  
 unreliability. The authors present a unified theory of reliability in future computational networks."*  
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- C<sub>217</sub> R.-M. Beiu, S. Hoara, and V. Beiu  
 And Now This: Hammocks for Quantum and Photonics  
 International Workshop on Soft Computing Applications SOFA 2020  
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- C<sub>216</sub> M. Tache, V. Dragoi, and V. Beiu  
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- C<sub>212</sub> M. Nagy, V. Dragoi, and V. Beiu  
Employing Sorting Nets for Designing Reliable Computing Nets  
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