VALERIU BEIU PROFESSOR

CONTACT INFORMATION

- "Aurel Vlaicu" University of Arad (UAV), Department of Mathematics & Computer Science
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SPECIALIZATION COMPUTER & ELECTRICAL ENGINEERING

- ***Bio-/brain-inspired nano-architectures (i.e., highly reliable & ultra low-power)***
  - Advanced VLSI (low power, reliability enhanced gates/circuits, novel communication schemes)
  - Digital design (including threshold logic)
  - Circuit & VLSI complexity
  - Hardware implementations of neural networks (including constructive neural learning)
  - Biological/neural computations and communication (including massively parallel architectures)
  - Computer architectures and computer arithmetic

BIO-SKETCH

I graduated in 1980 from the Computer Science & Engineering Department of the University "Politehnica" of Bucharest (Romania) with a MSc thesis on high-speed graphic workstations (*Best MSc Thesis Award*). I researched, designed and developed ultra high-speed floating-point units (FPUs) and central processing units (CPUs) for two years while with the Research Institute for Computer Techniques, Bucharest (Romania). Returning to the University "Politehnica" of Bucharest, I became Assistant Professor (1983), and Senior Lecturer (1990), teaching, researching (computer architecture, VLSI design, digital circuits, artificial neural networks), and supervising (29 MSc theses).

In 1991, being awarded both a *Fulbright Research Fellowship* (USA) and a *PhD Scholarship* (Belgium), I went for the doctoral studies, and have been on leave of absence from the University "Politehnica" of Bucharest (till 2001).

11/1991 – 11/1994 • PhD candidate with the Electrical Engineering Department, Katholieke Universiteit Leuven (Belgium), where in May 1994 I earned my *PhD summa cum laude* (*highest honors*) for a thesis on area- and time-efficient VLSI implementations of artificial neural networks using threshold logic gates.

12/1994 – 09/1996 • *Human Capital and Mobility Individual Research Fellow* of the European Union with the Centre for Neural Networks, King's College London (UK), conducting research on programmable neural arrays.

10/1996 – 08/1998 • *Director's Postdoctoral Fellow* with the Space and Atmospheric Sciences Division, Los Alamos National Laboratory (USA), investigating adaptive/reconfigurable field programmable neural arrays for deployable adaptive processing systems.

09/1998 – 05/2001 • *CTO and co-founder* of RN2R LLC and *Fellow* of Rose Research (Dallas, USA), coordinating research on ultra-fast low-power VLSI enabling neural-inspired gates and circuits.

From June 2001 I became an Associate Professor with the School of Electrical Engineering & Computer Science, Washington State University, involved in teaching (VLSI/nanoelectronics, ASICs/FPGAs, neural computations, computer architecture), researching (low-power and highly reliable VLSI circuits, emerging biological-inspired nano-architectures), and supervising (1 PhD and 2 MSc). In March 2005 I was offered a visiting professor position with the School of Intelligent Systems, University of Ulster (Londonderry, UK), and in July 2005 I joined the College of Information Technology (CIT), United Arab Emirates University (UAEU, Al Ain, UAE) as *Chair of Computer Engineering* (2005–2006), where in 2006 I was promoted to *Associate Dean for Research & Graduate Studies* (2006–2011) while also supervising (1 Postdoc and 2 MSc). Since Fall 2015 I joined "Aurel Vlaicu" University of Arad (UAV, Arad, Romania), where I started teaching in two graduate programs, advised 3 MSc, and leading a 2M€ research grant (2016–2020) while also supervising 2 PostDocs.

I am/was PI or co-PI on 44 grants/contracts ***totaling over 51 M$*** (as well as PI on 93 short-term travel grants). The research results have been published or accepted for publication: 2 books (3 more in slow progress), 8 book chapters (7 invited), 11 patents, 37 journal papers (3 invited), and 207 conference papers (27 invited and 7 best paper awards); presented over 400 times (out of which over 190 invited keynote/tutorials/presentations); and cited over 1470 times (excluding self-citations).

I have been a reviewer for the National Science Foundation (USA), the European Commission (EU), as well as for the science foundations of Romania, Belgium, Cyprus, Switzerland, UAE, as well as for many journals and conferences. I was an *Associate Editor* of the *IEEE Transactions on Neural Networks* (2005–2008), of the *IEEE Transactions on VLSI Systems* (2011–2015), and of the *Nano Communication Networks* (2010–2015). I have contributed to organizing over 120 international conferences and 11 invited workshops/sessions, chaired over 60 conference sessions, and I am a Senior Member of the IEEE since 1996 (in 1997 I was the Program Chairman of the IEEE Los Alamos Section), a founding member of the European Neural Network Society (ENNS), and a member of: the Association for Computing Machinery (ACM), the International Neural Network Society (INNS), the EU Marie Curie Fellowship Association (MCFA), and the American Nano Society (ANS). Additionally, I was a member of the SRC-NNI Working Group on Novel Nano-architectures (since 2003), the IEEE CS Task Force on Nano-architectures (since 2005), and the IEEE Emerging Technologies Group on Nanoscale Communications (since 2010).

ACCOMPLISHMENTS

"We know what we are, but know not what we may be." — *William Shakespeare*

DIRECTOR	• UAV	**BIOCELL-NANOART**	Arad	Romania	2016 – 2020
ASSOCIATE DEAN	• UAEU	CIT	Al Ain	UAE	2006 – 2011
CHAIR CE	• UAEU	CIT	Al Ain	UAE	2005 – 2006
FELLOWSHIPS	• Rose Research	Fellow	Dallas, TX	USA	1999 – 2001
	• Director's PostDoc	Fellow	Los Alamos, NM	USA	1996 – 1998
	• Individual Research	HCM Fellow (EU)	London	UK	1994 – 1996
	• Doctoral Research	Fellow	Leuven	Belgium	1991 – 1994
	• Fulbright Research	Fellow	—	USA	1991

PHD • Improved on the size/depth complexity for certain classes of Boolean functions

SUMA CUM LAUDE • Found novel VLSI-friendly constructive (learning) algorithms (similar to EDA-like synthesis)

PUBLICATIONS	• Books	2		(3 more in progress)
	• Chapters	8	7 invited	(5 more in progress)
	• Patents	11		(1 more in progress)
	• Journal papers (peer-reviewed)	37	3 invited	(6 more in progress)
	• Conference papers (peer-reviewed)	207	27 invited & 7 best paper awards	
	• Citations (excluding self-citations)	1474		
CONTRACTS	• Research grants/contracts	44		
OVER 51 M$	• Short-term travel grants	93		
TEACHING	• Advanced VLSI/Nanoelectronics, ASIC, Neural Computations, Neural Nets, Computer Architecture			
	• PostDoc (3), PhD (1), MSc (36)	40	5 UAV, 3 UAEU, 3 WSU, 29 UPB	

RESEARCH RELATED ACTIVITIES

- Referee for: National Science Foundation USA (8×), European Commission EU (6×), Belgium (2×), Cyprus (2×), Switzerland (2×), UAE (12×), and Romania (14×)
- Reviewer for: IEEE T. Nanotech., IEEE T. Neural Nets, IEEE T. Comp., IEEE T. Sys. Man & Cyber., IEEE T. CAD, IEEE T. Design & Test, IEEE T. VLSI, IEEE Access, ACM J. Emerg. Tech., Nanotech., Neural Nets., Neural Net. World, Neural Proc. Lett., Electr. Lett., etc.
- Associate Editor (2010 – 2015) Nano Communication Networks (Elsevier)
- Associate Editor (2011 – 2015) IEEE Transactions on VLSI Systems
- Associate Editor (2005 – 2008) IEEE Transactions on Neural Networks

• Best paper awards	7	
• Invited sessions/workshops	11	
• Invited articles in journals	3	
• Invited keynote/plenary	18	
• Invited tutorials	18	
• Invited lectures/seminars	46	
• Invited presentations (others)	115	(out of which 46 to industry)
• Organized international conferences	122	
• Chaired sessions at international conferences	62	

MEMBERSHIP

- Institute of Electrical and Electronic Engineers IEEE (*Senior Member* since 1996), International Neural Network Society (INNS), European Neural Network Society (ENNS, founding member), Association for Computing Machinery (ACM), EU Marie Curie Fellowship Association (MCFA)

MISCELLANEOUS

- *Four Gold Medals* (First Prize) at the National Physics Olympics
- *Best MSc Thesis Award*
- Expert of the European Artificial Neural Network Activity (DEANNA)
- Expert of the Romanian Academy of Sciences

CURRENT RESEARCH

- My current research activities are focused on nano-architectures, my major aim being to strengthen cooperation on *bio-/brain-inspired nano-architectures*, promote education, and generate new funding opportunities. This endeavor is based on a wide international cooperation, as quite a large number of researchers are actively pursuing nano-architectural initiatives. My hope is that, through direct collaboration (special sessions, visits, grants, etc.), the number of experts joining such efforts will grow. The ultimate goal is ***to advance understanding of enabling architectures*** which would match novel devices and associated communication schemes, performing research starting ***from ultra-low power reliability-enhanced bio-/brain-inspired circuitry up to large scale systems***.

EDUCATION

"Ability is of little account without opportunity." — *Napoleon Bonaparte*

POSTDOCTORAL

1996 – 1998	• LANL Director's Postdoctoral Fellow	Los Alamos National Lab
1994 – 1996	• EU Human Capital and Mobility (HCM) Individual Research Fellow	King's College London

PHD IN EE — SUMMA CUM LAUDE (HIGHEST HONORS) — KATHOLIEKE UNIVERSITEIT LEUVEN

1994 MAY	• Thesis	*Neural Networks Using Threshold Gates — A Complexity Analysis of Their Area- and Time-Efficient VLSI Implementations*		
1992	– Specialization	Neural Networks (course)	INST. UNIV. KURT BÖSCH	Certif.
1991	PhD exam	Parallel & Advanced Architectures	UPB	10/10
1990	PhD exam	Novel VLSI Structures	UPB	10/10
	PhD exam	Systolic & Neural Architectures	UPB	10/10
	PhD exam	Mathematical Complements	UPB	10/10
1989 MAY	– PhD entrance exam	*VLSI Efficient Implementations of Parallel Architectures*	UPB	10/10

MSC IN CE — BEST THESIS AWARD — UNIV. "POLITEHNICA" BUCHAREST

1980 JUNE	• MSc Thesis	*High-Speed Graphic Parallel Accelerators*	GPA 4.00/4.00	10/10
1979 DECEMBER	• BSc in CE		GPA 3.90/4.00	9.76/10

BACCALAUREATE — FIRST PLACE — "TUDOR VIANU" COLLEGE OF IT

The Diploma of Baccalaureate states that I am a *"programmer and software assistant analyst"*

1975 GRE EQUIV.	• Final examination (Baccalaureate)	GPA 3.84/4.00	9.60/10
1975	• *First place (highest GPA) at graduation*	GPA 3.70/4.00	9.26/10

ALMA MATERS

University "Politehnica" of Bucharest – Founded in 1818, it is the largest technical university of Romania with over 28,000 students (www.upb.ro/en/). The Computer Science & Engineering Department (CSE) was founded in 1969 (cs.pub.ro/) by Prof. Mircea Petrescu.

Katholieke Universiteit Leuven – Founded in 1425, is the oldest catholic university of Northern Europe, recognized for names like Erasmus, Mercator, and Vesalius (www.kuleuven.be/english/), is *in the world's top 100 universities* (***47*** in THE, ***71*** in QS – World University Rankings 2018), and is the largest university in Belgium. The EE Department of was founded in 1900 (www.esat.kuleuven.be/index.en.php).

King's College London – Founded in 1829, is one of the larger and oldest of London (www.kcl.ac.uk), with about 23,000 students, and is *in the world's top 100 universities* (***36*** in THE, ***23*** in QS – World University Rankings 2018). The Mathematics Department (www.kcl.ac.uk/nms/depts/mathematics/) has received the highest rating in the Research Assessment Exercise, being a 'center of excellence'. The *Centre for Neural Networks* was the coordinator of the *European Neural Networks Network of Excellence*.

ADVISORS

Prof. Mircea Petrescu – Founder of the CSE Department, Vice-Provost, and Director of the Computer Center, State Secretary of the Government of Romania, as well as Visiting Professor at the University of California at Berkeley (USA) and at the University of Grenoble (France). He was Vice-President of the Romanian Academy of Technical Sciences and is an honorary member of the Romania Academy of Sciences. He has published more than 120 articles and 8 books. http://ro.wikipedia.org/wiki/Mircea_Petrescu

Prof. Joos Vandewalle – Has been Vice-Dean, Visiting Professor at the University of California at Berkeley (USA), Chairman of the EE Department, and holder of the Francqui Chair on Neural Networks at the University of Liege (Belgium). He was elected Fellow IEEE in 1992, and Fellow IEE in 1998, and was the Vice-President for Region 8 of the IEEE Society on Circuits & Systems, and the coordinator of the Center for Neural Networks (Belgium). He has published over 600 articles and 18 books. http://www.esat.kuleuven.be/stadius/person.php?id=18

Prof. John G. Taylor – Has been Director of the Centre for Neural Networks and President of the International Neural Network Society. He has held positions at: Institute of Advanced Study, Princeton (USA); Institut des Hautes Etudes, Paris (France); Christ College, Cambridge (UK); Mathematics Institute, Oxford (UK); Physics Department, Southampton (UK); Queen Mary College, London (UK); Rutgers University, New Jersey (USA). He has published more than 400 articles and over 20 books. http://en.wikipedia.org/wiki/John_G._Taylor

POSITIONS HELD	DATES	INSTITUTION	ADDRESS
PROFESSOR	• **09/2015 –**	**"Aurel Vlaicu" University Faculty of Exact Sciences**	**Str. Elena Dragoi nr. 2-4 RO-310330 Arad, Romania**
Professor	08/2008 – 08/2015	UAE University	Maqam Campus, Bldg. E1
Associate Dean	08/2006 – 08/2011	College of IT	PO Box 15551, Al Ain, UAE
Chair CE	07/2005 – 08/2006		
Visiting	03/2005 – 08/2011	University of Ulster	Londonderry, UK
	07/2003 & 08/2004	Heinz Nixdorf Institute	Paderborn, Germany
	07/2002 & 04/2008	Los Alamos National Lab. Theoretical Division	MS 319, Los Alamos NM 87545, USA
Associate Professor	06/2001 – 06/2005	Washington State Univ. School of EECS	Spokane 102, Pullman WA 99164, USA

Co-founder • 05/1998 –	RN2R LLC	Merit Drv.12750, #1020
CTO/Fellow 09/1998 – 05/2001	Rose Research	Dallas, TX 75251, USA
Director's 10/1996 – 08/1998	Los Alamos National Lab.	MS D466, Los Alamos
PostDoc Fellow	Division NIS	NM 87545, USA
EU HCM 12/1994 – 09/1996	King's College London	Strand, London
Res. Fellow	Centre for Neural Networks	WC2R 2LS, UK
Res. Fellow 05/1994 – 11/1994	Katholieke Univ. Leuven	Kasteelpark Arenberg 10
PhD cand. 11/1991 – 05/1994	EE Dept., ESAT-ACCA	Leuven, B-3001 Belgium
Co-founder • 04/1990 –	SPRING Software Consult SRL	Blvd. Magheru 20, Bucharest
President 04/1990 – 08/1991		RO-10721, Romania
Senior Lect. 01/1990 – 06/2001	Univ. "Politehnica" of	Spl. Independentei 313, Bucharest
Assist. Prof. 01/1983 – 12/1989	Bucharest, CSE Dept.	RO-10334, Romania
Senior Res. 09/1981 – 01/1983	Research Institute for	Cl. Floreasca 167/9, Bucharest
Res. Eng. 09/1980 – 08/1981	Computer Techniques	RO-14459, Romania

TEACHING

"I like to learn, but I don't like to be taught" — *Winston Churchill*

I have been teaching/lecturing since 1981. Between 1981 and 1983 I have been teaching part time, while since 1983 I have been teaching full time in the Computer Science & Engineering (CSE) Department of the University "Politehnica" of Bucharest (UPB): Assistant Professor (1983–1990), and Senior Lecturer (1990–2001). Between 1984 and 1991 I supervised 29 MSc candidates. Between 2001 and 2005, I was with the School of Electrical Engineering & Computer Science (EECS), Washington State University (WSU), where I supervised two MSc and one PhD, and contributed to getting the ABET accreditation of the newly formed Computer Engineering program. In 2005 I joined the College of Information Technology (CIT), United Arab Emirates University (UAEU), as well as visiting professor with the University of Ulster (UU). At UAEU I contributed to the ABET accreditation of the CIT, which started offering MSc in Fall 2013. That is why, since joining UAEU (in 2005), my graduate supervision has been limited to: invitations on 8 PhD evaluation committees, co-supervising 2 MSc, and advising 1 PostDoc. Since Fall 2015 I am involved with two graduate programs offered by the "Aurel Vlaicu" University of Arad (UAV) having advised 3 MSc, while currently I am supervising 2 PostDocs. Additionally, I have given 18 invited tutorials and 46 invited seminars/lectures.

	COURSES TAUGHT/DEVELOPED	SINCE	UPB	WSU	UAEU	UAV
UNDERGRADUATE	– Hardware Testing & Fault Tolerance	2013			UAEU	
	– Professional Responsibility in IT	2012			UAEU	
	– Advanced Computer Architecture	2006			UAEU	
	– ASIC & Digital Systems/VLSI Design	2001		WSU	UAEU	
	– Introduction to Algorithms/Programming	1984	UPB			UAV
	– Digital Computer Architecture	1983	UPB		UAEU	
	– Analysis & Synthesis of Digital Circuits	1981	UPB		UAEU	
GRADUATE	– Neuro-Bio Fundamentals	2015				UAV
	– Research Methods in IT	2011			UAEU	UAV
	– Advanced VLSI/Nanoelectronics	2004		WSU		
	– Neural Computations	2003		WSU		UAV
	– Neural Networks & Applications	1990	UPB	WSU		
	– VLSI Design & Applications	1983	UPB			UAV
	– Advanced Computer Architecture	1983	UPB			
	– Testing & Performance Evaluation	1982	UPB			

STUDENTS EVALS. • Constantly higher (avg. **4.65/5.00**) than college (CIT 4.48/5.00) and university (UAEU 4.41/5.00)

		GRADUATE SUPERVISING	UAV (5), UAEU (3), WSU (3), UPB (29)	
2018	40	– Using Deep Learning for Data Analysis	Ionel Mazilu	MSc
	39	– On the Reliability of Critical Networks	Dan-Cristian Pascu	MSc
	38	– 3D Fibonacci Spirals	Beniamin-Otniel Voian	MSc
	37	– Optimizing Two-terminal Networks Using Compositions	Vlad Dragoi	**PostDoc**
2017	36	– Hammock Networks and Generalizations	Simon R. Cowell	**PostDoc**
2013	35	– Monte Carlo Analyses of XOR-2 in 22/16nm PTM (BITS Pilani)	Nilay V. Acharya	MSc
	34	– Monte Carlo Analyses of MAJ-3 in 22/16nm PTM (BITS Pilani)	Jithu Lissi Raju	MSc
2012	33	– Brain-inspired Interconnects for Nanoelectronics	Pietro Santagati	**PostDoc**
2004	32	– Design & Analysis of SET: Neural-Inspired Gates & Circuits	Mawahib H. Sulieman	**PhD**
	31	– Optimizing the Performance of Direct Digital Frequency Synthesizers for Low-Power Wireless Communication	David Betowski	MSc
2003	30	– Precise Sine Approximations with Reduced Resources	Pao-Szu Wu	MSc
1991	29	– Simulator for the Implied Minterm Structure	Simona Ivanov	MSc
1990	28	– Set of C Functions for Simulating Parallel Processes	Dinu Creteanu	MSc
	27	– Graphic Interface for a Neural Network Simulator	Dan Stoicescu	MSc
	26	– Microbusiness Software Package	Anca Costin	MSc
	25	– Neural Network Arithmetic Logic Unit	Yousuf Basmark	MSc
	24	– VLSI Parallel Architecture for Histogram Modification	Aida Gheorghiu	MSc
	23	– Boltzmann Machine Simulator	Mihaela Dumbrava	MSc
	22	– Neural Network Solutions to Optimization Problems	Orest Robciuc	MSc
	21	– Motion Detection Using Neural Networks	Anca Sigala	MSc
	20	– Enhanced VLSI CAD Package	Daniel Mandu	MSc
1989	19	– Recognition of Characters Using Neural Networks	Abdel Nehad	MSc
	18	– Neural Network Medical Expert System	Sima Gheorghita	MSc
	17	– VLSI Animated Lesson for PC	Şerban Benone	MSc
1988	16	– Neural Network Simulator	Sobhui Darwish	MSc
1987	15	– VLSI CAD Tool: Place & Route	Anca Şerban	MSc
	14	– VLSI CAD Tool: Interactive Layout	Mariana Mirea	MSc
1986	13	– Computer Interface for a Rotating Magnetic Head Unit	Sorinel Ciobanu	MSc
	12	– CAD Tool for Digital Image Segmentation	Cornelia Ciotînga	MSc
	11	– CAD Tool for Digital Image Enhancement	Mihai Dinu	MSc
1985	10	– Systolic Floating Point Coprocessor: Multiplication & Division	Eugen Paşol	MSc
	9	– Systolic Floating Point Coprocessor: Addition & Subtraction	Liviu Zuzu	MSc
	8	– VLSI Ultra High-Speed Arithmetic Units	Marius Ionescu	MSc
	7	– Dedicated Serial Data Multiplier	Daniel Manica	MSc
	6	– Systolic Circuits for Convolution	Anca Tanga	MSc
	5	– A Study of Permutation Networks for VLSI Implementation	Sorin Tene	MSc
1984	4	– VLSI Rule Checking Expert System	Manuela Anton	MSc
	3	– High Speed Arithmetic Units	Bianca Tudor	MSc
	2	– Self-Testable RAM/CAM Memory	Cristina Borş	MSc
	1	– Self-Testable & Self-Repairable Correlation Circuit	Irina Manole	MSc

PLANS FOR COURSE DEVELOPMENT

ADVANCED VLSI/ NANOELECTRONICS

- Novel nano-devices, new design styles, reliability enhancements, and reconfigurable computing

Examples http://bwrcs.eecs.berkeley.edu/Classes/icdesign/ee241_s13/
http://www.cisl.columbia.edu/courses/spring-2002/ee6930/reader.html
http://www.ece.unm.edu/~jimp/vlsiII/index.html
http://www.ece.utah.edu/~harrison/lpdocs/ [not active anymore]

ELECTRONIC NANOTECHNOLOGY

- This course could precede **ADVANCED VLSI/NANOELECTRONICS**

Examples https://nanohub.org/courses/NT
http://www-2.cs.cmu.edu/afs/cs/academic/class/15849c-s02/www/schedule.htm
http://www.eng.fsu.edu/~mpf/PhysLim/

RECONFIGURABLE COMPUTING

- Introduces 'future/beyond FPGA' based on nano-devices (http://www-2.cs.cmu.edu/~phoenix/).

Examples http://www.ecs.umass.edu/ece/tessier/courses/636/index.html
http://www.cs.cmu.edu/afs/cs.cmu.edu/academic/class/15828-s98/www/index.html

DIGITAL COMPUTER ARITHMETIC

- Classic course bridging algorithms and hardware; could be based on the books of Ercegovac & Lang http://www.cs.ucla.edu/digital_arithmetic/ and Koren http://www.ecs.umass.edu/ece/koren/arith/

Examples http://web.cs.ucla.edu/~milos/CSM51A-W17-Syllabus.pdf
http://web.cs.ucla.edu/~milos/CS252A-S17-INTRODUCTION.pdf
http://lap.epfl.ch/courses/ [PhD course "Computer Arithmetic" not available anymore]
http://users-tima.imag.fr/cis/guyot/Cours/Oparithm/ [not active anymore]

BIO-/BRAIN-INSPIRED COMPUTATIONS & COMMUNICATIONS

- This course will go on to cover the digital-to-analog divide as well as parallel-and-neural computing architectures, learning and the power-reliability-communication design tradeoffs

Examples http://www.ece.jhu.edu/~andreou/761/ & http://www.ece.jhu.edu/~andreou/762/
http://seunglab.org/courses/

RESEARCH

"Never lose a holy curiosity." — *Albert Einstein*

EXPERIENCE

- ***I was involved in research for 39 years, holding management positions for over 20 years, and executive positions for more than 10 years.***

EXPERTISE

- My expertise encompasses a range of areas starting from circuit/VLSI complexity, going through information theory, optimization techniques, and neural computations, to advanced VLSI/ nanoelectronics and adaptive/reconfigurable circuits and systems.

INTERESTS

- I like to take abstract concepts for difficult but practical applications, turn them into efficient algorithms, and then design innovative VLSI circuits performing them optimally (e.g., at ultra-high speeds, with very low power/energy, highly reliable, etc.). I am extremely interested by emerging nanoelectronics and in particular by bio-/brain-inspired nano-architectures (massively parallel, adaptive/reconfigurable, fault-tolerant, using alternate communication schemes), and by their optimized designs inspired by arrays (e.g., biological/ion-channels, cellular, systolic).

SIGNIFICANT RESEARCH RESULTS (FIRST EVER)

- ***Advancing understanding of reliability for (classes of) two-terminal networks*** 2017 –
- ***Generalizations of hammock nets to 3D (akin to axonal transport networks)*** 2017 –
- ***Energetics of neural communication (over $10^3\times$ lower energy than CMOS)*** 2015 –
- ***Reliability of hammock nets (over $10^{10}\times$ better than von Neumann multiplexing)*** 2015 –
- Reported the best lower and upper bounds for consecutive-*k*-out-of-*n* systems 2014
- Designed ultra low-power hybrid NEMS-CMOS circuits 2014
- Analyzed Schmitt trigger gates/circuits (performances vs. applications) 2013
- Detailed & accurate Monte Carlo simulations using Predictive Technology Models 2013
- Highly reliable and low power CMOS circuits based on novel enabling sizing of transistors 2012

- Low-power and highly reliable bio-inspired arrays for communication and computation 2010
- Axon-inspired redundancy scheme ($10^3\times$ better than von Neumann multiplexing) 2009
- Bayesian EDA tool for very accurate reliability estimates (devices, input vectors, wires) 2009
- Introduced & evaluated NOR-2 von Neumann multiplexing 2010
- Estimated wires' reliability due to intrinsic noises (shot, thermal) 2009
- Used Rent rule to explain Brain's columnar structures (optimal hierarchical networks) 2007
- Devices & input vectors are more important than gates (when evaluating reliability) 2007
- Showed that serial connected architectures are optimal for nanoelectronics 2005
- Designed and simulated single electron transistor gates & circuits considering variations 2005
- Designed & simulated the largest single electron transistor circuit 2004
- Exact calculations of the reliability of von Neumann multiplexing (gate-level) 2004
- Proposed novel highly reliable and low-power locally connected architectures 2004
- Highly accurate piecewise linear, non-linear, and hybrid ROM-less DDFS 2003
- Noise-robust low power (self-timed, charge recycling, sub-threshold) perceptrons 2000
- Designed ultra-high performance adders using Fibonacci-weighted threshold gates 1999
- Showed that deeper & sparser artificial neural nets are VLSI-optimal 1997
- The best/tightest circuit complexity bounds for feed-forward neural computations 1994
- Proposed a continuous version of the Boltzmann machine 1992
- Self-testable and self-repairable units are a must for VLSI 1984

HISTORY

1979 – 1989
- My research has been centered on *digital VLSI*, and in particular on: high-speed processing units (ALUs), smart memories (e.g., content addressable, set processing, hierarchical, self-testable), regular arrays (e.g., systolic, cellular). On these topics I have published about 20 papers. Since 1985 I have started looking into neural networks. This shift of interest was clearly marked by the paper "From Systolic Arrays to Neural Networks," *Scientific Annals of Al. I. Cuza Univ.*, 35(4):375–385, 1989 (J_3).

1985 – 1992
- I have been 'learning' about *neural networks*, publishing about their capabilities (for image enhancement and recognition), and delved into Boltzmann machines introducing the new concept of a *continuous Boltzmann machine* (C_{28}). On these topics I have published about 10 papers.

1992 – 2002
- I have been working on *hardware/VLSI implementations of threshold logic gates (perceptrons)*. On these topics I have published about 80 papers. This direction of research can be subdivided into:
  – *constructive learning* algorithms (equivalent to CAD/EDA synthesis, e.g., based on decomposition of functions, using the entropy of the data set, based on Kolmogorov's superpositions, etc.);
  – theoretical *circuit/VLSI complexity* issues;
  – hardware implementations (e.g., mapping onto FPGAs);
  – VLSI implementations (e.g., high-speed, low-power, reliability enhanced, noise immune).

SINCE 2003
- I have been focusing on *nano-architectures*. On this topic I have published over 160 papers:
  – ultra low-power and reliability-enhanced (gates, circuits and systems);
  – from von Neumann multiplexing to novel array-based redundancy schemes (e.g., axon-inspired);
  – brain-inspired hierarchical optimal interconnect topologies/networks;
  – analyses of wires and alternate communication paradigms.

RESULTS
- ***Funded*** ***44 research grants/contracts, and 93 short-term travel grants*** **51 M$**

Published 2 books, 8 chapters, 11 patents, 37 journals, 207 conferences
Invited 18 keynotes, 18 tutorials, 46 lectures, 115 presentations (out of which 46 to industry)
Cited 1474 times (excluding self-citations, hand counted and available upon request)
Organized 122 conferences, 62 sessions chaired

RESEARCH PROJECTS/GRANTS (AWARDED, DIRECTED, ETC.)

In planning	– TBD [EU COST Action] — With S. Lazarova-Molnar (U Southern Denmark)	Co-PI	
In planning	– EDA for NEMS and Reliability-Optimal CMOS-transistor Sizing (EDA-ROCS) With W. Ibrahim (UAEU), and T.-J. King Liu (UC Berkeley)	Co-PI	
In preparation	– Ultra Reliable Array-based Architectures for CMOS and Beyond (URA^2) With L. Anghel (INP Grenoble), NanoSciences Foundation	PI	1M€
In preparation	– Novel Biologically-inspired Architectures for nano-Devices (NBAD) With G. Fettweis (TU Dresden), EU ERC Advanced	PI	3M€
2018	• Short term travel grants (invited): ICCCC'18 (US$ 1000), SOFA'18 (US$ 600)		1.6K$
2016 – 2020 **BIOCELL-NANOART**	• **Novel Bio-inspired Cellular Nano-architectures** With V.-F. Duma (UAV), F.-D. Munteanu (UAV), C. Stoica (UAV), P. Gaspar (UAV), V.E. Balas (UAV), M. Balas (UAV), A. Cavaco-Paulo (U Minho), L. Daus (UTC Bucharest)	PI POC-A1-A1.1.3-E nr. 30/2016	9.3MRON
2016	– Short term travel grants (invited): ICCCC'16 (US$ 500), SOFA'16 (US$ 500) IEEE-NANO'16 (US$ 1,000)		2K$
2014 – 2016 ULP-DigiFinA	– ATIC-SRC Center of Excellence in Energy Efficient Electronic Systems (ACE^{4}S) Task: Ultra-low Power Digital Sub-threshold FinFET Amplifiers Originally with G. Fettweis (TU Dresden) and M. Alioto (Natl. U Singapore) https://www.src.org/newsroom/press-release/2013/452/	Co-PI SRC GRC ACE^{4}S	35MAED
2013 – 2016 SECRET	– Strengthening Research Collaborations in High-impact and Emerging Technologies between GCC and EU With *B. Aziz M. Rahman* PI (City U London), G. Cuniberti (TU Dresden), V. Hessel (TU Eindhoven), O. Benitez (U Deusto), P. Candeloro (U Magna Graecia), C. Themistos (Frederick U), H. Bourdoucen (Sultan Qaboos U), F. Bou-Rabee (Kuwait U), S.A. Al-Mansoori (U Bahrain), F. Kharbash (UAEU)	Co-PI EU EM 545790-EM-1-2013-1-UK-ERA MUNDUS-EMA22	1.23M€
2012 – 2015 SYMONE	– Synaptic Molecular Networks for Bio-inspired Information Processing With *G. Wendin* PI (Chalmers U), D. Vuillaume (CNRS-IEMN), J. Roncali (CNRS-MOLTECH), M. Calame (Basel U), S. Yitzchaik (HUJI), C. Gamrat (CEA), and G. Cuniberti (TU Dresden)	Co-PI EU FP7-ICT-318597	2.81M€
2012 – 2014 Use-LP	– Unconventional Sizing for Enabling Low Power Digital Design With M. Alioto (U Siena/Natl. U Singapore), A. Beg (UAEU), W. Ibrahim (UAEU), and F. Kharbash (UAEU)	PI SRC 2012-TJ-2332	200K$
2011 – ULP-NBA	• Ultra Low-Power Application-specific Non-Boolean Architectures [Intel Co] With *Intel* PI, D. Hammerstrom (Portland State U), W. Porod (U Notre Dame), S.P. Levitan (U Pittsburgh), T. Shibata (U Tokyo), T. Roska (Hungarian Acad. Sci.), M. Pufall (NIST), D. Weistein (MIT), and M.R. Stan (U Virginia)	Co-PI URO 2011-05-24G	1M$
2011 – 2015 ULP-NEMS-CMOS	– Ultra Low Power NEMS-CMOS With T.-J.K. Liu (UC Berkeley), W. Ibrahim (UAEU), and A. Beg (UAEU)	PI SRC 2011-HJ-2184	300K$
2011 – 2013	– Brain-inspired Interconnects for Nanoelectronics (BiIN) With W. Ibrahim (UAEU) [UAE Natl. Res. Found.]	PI NRF 1108-00451	586KAED
2011 – 2013	– Algorithms & EDA for Accurate Nano-Circuits Reliability Calculations (CREDA^2) With *W. Ibrahim* PI (UAEU) [UAE Natl. Res. Found.]	Co-PI NRF 1108-00329	506KAED
2013	– Short term travel grants (invited): TUDresden (US$ 7,000)		7K$
2012	– Short term travel grants (invited): EDCC'12 (US$ 1,000)		1K$
2011	– Short term travel grants (invited): IEEE-NANO'11 (US$ 500), EU Brussels (US$ 8,000), EU Paris (US$ 5,000), NSF (US$ 5,000), ATIC-SRC (US$ 10,000)		28.5K$
2011 – 2012	– Brain-inspired Hybrid Topologies for Nano-architectures [SRC 2011-RJ-2150G]	PI	40K$

2010	– Short term travel grants (invited): IDT'10 (US$ 500), IJCNN'10 (US$ 1,500), INC6 (US$ 1,000), MEES'10 (US$ 3,000)		6K$
2009 – 2011	– Brain-inspired Interconnects for Nanoelectronics [British Council PMI2 RCGS271]	PI	39KUK£
2009 [on hold]	– Emirates Center for Nanoscience & Nanoengineering [UAE Natl. Res. Found.] http://www.thenational.ae/news/uae-news/education/grant-aids-research-centres	Co-PI	50MAED
2009	– Short term travel grants (invited): EU (US$ 7,000), U Oslo (US$ 5,000), IEEE-NANO'09 (US$ 1,000), ESSCIRC'09 (US$ 1,500), NanoNet'09 (US$ 1,000), WDSN'09 (US$ 5,000)		20.5K$
2008	– Short term travel grants (invited): NSF (US$ 5,000), LANL (US$ 2,000), SAMOS VIII (US$ 5,000), Tohoku U (US$ 10,000), U Paris-Sud (US$ 3,000), U Oslo (US$ 5,000)		33K$
2007	– Short term travel grants (invited): NSF (US$ 5,000), EU (US$ 8,000), HP Labs (US$ 6,000), FENA/UCLA (US$ 1,000), ULSIWS'07 (US$ 400), ISMVL'07 (US$ 1,000), SHARCS'07 (US$ 2,000), DTIS'07 (US$ 3,000), DCIS'07 (US$ 3,000), IECON'07 (US$ 3,000), Tohoku U (US$ 5,000), MWSCAS'07 (US$ 1,000), IEEE-NANO'07 (US$ 1,000), ICSPC'07 (US$ 500), ICTRF'07 (US$ 500), IDT'07 (US$ 500), IWANN'07 (US$ 5,000), NanoMaterials'07 (US$ 500), Univ. Oslo (US$ 5,000)		51.4K$
2006 – 2011	– Center for Excellence in Intelligent Systems [InvestNI, IDF and U Ulster] Center for Neural Inspired Nano Architectures (~1.8MUK£, 2007–2010)	Co-PI	20.4MUK£
2007	– Mapping the proxel method to reliability analysis of nanoarchitectures [UAEU]	Co-PI	8KAED
2006	– Short term travel grants (invited): NSF (US$ 5,000), WNEC'06 (US$ 2,500), IDT'06 (US$ 500), AICCSA'06 (US$ 500)		8.5K$
2006	– Investigation of the reliability of single electron technology gates & circuits [UAEU]	Co-PI	8KAED
2005	– Short term travel grants (invited): ICM'05 (US$ 3,000), U Ulster (US$ 9,000), SNB'05 (US$ 3,000), IIT'05 (US$ 1,000)		16K$
2005 – 2006	– Defect-tolerant high-performance low-power computing with hybrid CMOS molecular circuits [Advanced Research & Development Agency, ARDA]	Co-PI	100K$
2004	– Short term travel grants (invited): ASAP'04 (US$ 500), NGCM'04 (US$ 1,000), IJCNN'04 (US$ 500), Heinz Nixdorf Inst. (US$ 1,500)		3.5K$
2003	– Short term travel grants (invited): MWSCAS'03 (US$ 500), ICNNSP'03 (US$ 500), NIPS'03 (US$ 500), U Paderborn (US$ 1,500), IJCNN'03 (US$ 500), IWANN'03 (US$ 500), NCI'03 (US$ 500), Heinz Nixdorf Inst. (US$ 2,000)		6.5K$
2002 – 2004	– Direct Digital Frequency Synthesizers (DDFSs) for reconfigurable communication systems. DDFSs have been investigated and implemented in silicon-on-insulator (SOI) and CMOS for space applications [Air Force Research Lab/CDADIC]	Co-PI	250K$
2002	– Short term travel grant (invited): LANL, Los Alamos (US$ 5,000)		5K$
2001	– Short term travel grant (invited): Berkeley Wireless Research Center (US$ 4,000)		4K$
2000 – 2003	– Conducting research on ultra-fast low-power floating point units (FPUs), with applications to graphic accelerators and gaming workstations [Rose Research]	PI	500K$
2000 – 2003	– Evaluating/examining solutions for ultra-fast low-power en/decryption allowing for wire-speed (i.e., on-the-fly) crypto-processors [Rose Research]	PI	500K$
1999 – 2005	– Pioneered *FastLogic*, an enabling VLSI technology based on novel ultra-fast logic gates, and a systematic design methodology for using them. Low-power was achieved by means of a novel self-timed power-down mechanisms, as well as differential (charge recycling) circuits. Several versions of *FastLogic* gates have been designed, simulated, tested, and patented (during 1999-2001). Ultra-low power sub-threshold versions have also been designed using an original cross-coupled adaptive body biasing scheme for boosting reliability. [Rose Research]	PI	3M$
1999 – 2002	– Exploring alternatives and improving on ultra-fast low-power multiplication and multiply-accumulate with application to digital signal processing [Rose Research]	PI	1M$
1999	– Short term travel grant (invited): AMS-SMM'99 (US$ 500)		0.5K$

1998 – 1999	– Researched, analyzed and enhanced ultra-fast VLSI adders. The theoretical results obtained have been verified and patented. [Rose Research]	PI	500K$
1998	– Short term travel grants (invited): NC'98 (US$ 500), CNRS-Paris (US$ 1,000), PARELEC'98 (US$ 500), EIS'98 (US$ 1,000)		3K$
1997	– Short term travel grants (invited): SBRN'97 (US$ 5,000), IDIAP, Switzerland (US$ 2,000), Heinz Nixdorf Inst. (US$ 1,500), U Paris XII (US$ 1,000), Royal Holloway U (US$ 1,000), Oxford U (US$ 1,000), NEuroTop'97 (US$ 600)		12.1K$
1996 – 1998	– Field Programmable Neural Arrays (FPNAs) as a component of the Deployable Adaptive Processing Systems (DAPS) [Los Alamos National Lab]	PI	180K$
1996	– Short term travel grants (invited): ANITA'96 (US$ 1,500), SBRN'96 (US$ 2,500), AT'96 (US$ 500)		4.5K$
1995	– Short term travel grants (invited): ADT'95 (US$ 500)		0.5K$
1994 – 1996	– Programmable Neural Arrays, Design & VLSI Implementation of Neural Networks Using Threshold Gates [EU CHBICT941741]	PI	440K$
1994	– Short term travel grants (invited): ConTI'94 (US$ 300), EMCSR'94 (US$ 300), RRCS'94 (US$ 500)		1.1K$
1993	– Short term travel grants (invited): ROSYCS'93 (US$ 300), ESSAN'93 (US$ 600)		0.9K$
1992	– Short term travel grant (invited): EPFL (US$ 500)		0.5K$
1991	– Short term travel grants (invited): ICIAM'91 (US$ 1,500), ICANN'91 (US$ 1,500)		3K$
1990 – 1991	– Negotiated, won, managed, and coordinated SPRING Software Consult contracts		
	» Dedicated En/Decryption and GUI [Ministry of National Defense]	PI	20K$
	» CAD Training (lectures) [AVERSA SA]	PI	5K$
	» Software Package for Microbusiness [Chemistry Research Institute]	Co-PI	10K$
	» Data Acquisition CAD Package [Chemistry Research Institute]	PI	10K$
	» PC Training (lectures) [Ministry of National Defense]	PI	5K$
1990	– Short term travel grant (invited): PARCELLA'90 (US$ 300)		0.3K$
1988	– Dedicated watch-dog system: Feasibility study & reliability analysis [Electrical Networks Institute]	PI	50K$
1987 – 1988	– Studied and analyzed Prolog as a research tool for circuit simulations [UPB]	Co-PI	
1987	– Short term travel grant (invited): ComEuro'87 (US$ 400)		0.4K$
1987	– Dedicated Database Package [National Information & Documentation Institute]	PI	50K$
1987	– Hierarchical Self-testable and Self-repairable Content Addressable Memory [UPB]	PI	50K$
	– High Speed Antialiasing Cascadable Circuit [UPB]	PI	50K$
1984 – 1987	– VLSI CAD Package (PC version) [UPB]	PI	100K$
	– Automatic Conical Ball Bearing Sorter [Bearings Factory Alexandria, now Koyo]	PI	100K$
1983	– Mutual exclusion circuit (patented) [Research Institute for Computer Techniques]	PI	
	– Floppy disk interface [Research Institute for Computer Techniques]		
1981 – 1982	– Ultra high-speed floating point unit. New improved algorithms with innovations at the microprogramming level [Research Institute for Computer Techniques]	PI	
1981	– Ultra high-speed highly reliable central processing unit with enhancements at the microprogramming level [Research Institute for Computer Techniques]	PI	
1980	– Involved in the final testing stages of the CE-100 computer (PDP equivalent)	Co-PI	
1979 – 1980	– High speed graphic workstation: 1024×1024 with 16 intensities [UPB]		5K$
	20 MHz HP vectorial display and original CPU design (tested at 60 MHz)		
	» Three Best Paper Awards at the Students' Scientific Research Conference		
	» Best MSc Thesis Award for *"innovations in workstation design"*		
1977 – 1980	– National Merit Scholarship [Ministry of Science & Education]		10K$

Research participated

1996 – 1998 – The Deployable Adaptive Processing Systems (DAPS) carried out at Los Alamos National Laboratory (LANL). This was a multi-faceted R&D program, developing algorithms and prototyping systems for real-time remote and autonomous processing of data gathered on land, in the air, or in space. Specified and designed neural-inspired adaptive algorithms and their mapping onto FPGAs.

1992 – 1994 – VLSI-efficient threshold logic gates (Concerted Research Action of the Flemish Community).

1991 – One of the experts of DEANNA (Data-base for European Artificial Neural Network Activity), an ESPRIT exploratory action led by JENNI (Joint European Neural Network Initiative).

Other research related activities

11 Patents

- 7 USA (2001-2003), 3 Taiwan (2002), 1 Romania (1984) — ***single author on all of them***

122 Conferences Organized

- RRCS'94, ANITA'96, NEuroFuzzy'96, NeuroTop'97, SBRN'97, EIS'98, SOCO'99, EIS'00, SBRN'00, IWANN'03, NCI'03, IJCNN'04, IJCNN'05, NanoArch'05, IDT'06, IEEE-NANO'06, IEEE SoC'06, IJCNN'06, NanoArch'06, WSC-11, ICMENS'06, IDT'07, IIT'07, IEEE SoC'07, IJCNN'07, MCSoC'07, NanoArch'07, WSC-12, DCS'08, IDT'08, MIM-MMN'08, NanoArch'08, NDCS'08, VTS'08, WSC-13, DTIS'09, ICMLA'09, IJCNN'09, MIM-MMN'09, NanoArch'09, NanoNet'09, WSC-14, BCN'10, BIONETICS'10, ICTITA'10, IDT'10, MIM-MMN'10, MCSoC'10, NanoArch'10, NaNoNet'10, SBCCI'10, WAC'10, WSC-15, ICMLA'11, IDT'11, MIM-MMN'11, MoNaCom'11, NaBIC'11, NanoArch'11, SBCCI'11, ISIE'12, MIM-MMN'12, MoNaCom'12, NaBIC'12, NanoArch'12, OPTIM'12, SBCCI'12, WICT'12, WSC-16, DTIS'13, ICECS'13 (*track chair*), IDT'13, IIT'13, IJCNN'13, MIM-MMN'13, MoNaCom'13, NanoArch'13, SBCCI'13, VLSI-SoC'13, BICT'14, BioTL'14, DTIS'14, I4CT'14, ICECS'14 (*track chair*), ICNC'14, IIT'14 (*chair*), IDT'14, ISCAS'14, MIM-MMN'14, NanoArch'14, NanoCom'14, SBCCI'14, SSCI'14, WSC-18, DTIS'15, ECCTD'15, ICECS'15 (*track chair*), IDT'15, IJCNN'15, MIM-MMN'15, NaBIC'15, NanoArch'15, NanoCom'15, SBCCI'15, SSCI'15, DTIS'16, ICCCC'16, ICECS'16 (*publicity chair*), IDT'16, ISCAS'16, MIM-MMN'16, SETIT'16, SOFA'16, DTIS'17, ICLM'17, ISCAS'17, ISPACS'17, SoCPaR'17, ICCCC'18, ISREIE'18, DTIS'18, SOFA'18

62 Sessions Chaired

- CSCS'93, ROSYCS'93, RRCS'94, ConTI'94, ADT'95, CSCS'95, IWANN'95, NeuroTop'97, CSCS'97, EANN'97, SOCO'97, EIS'98 (2×), PARELEC'98, NC'98, ISCAS'00, MWSCAS'00 (2×), NCI'03 (2×), IWANN'03, ICANN'03, SCS'03, IJCNN'03, NIPS'03 (2×), MWSCAS'03, IJCNN'04 (2×), IJCNN'05, IIT'05, VLSI-SoC'05, ICM'05, AICCSA'06 (2×), IIT'06, ISMVL'07, IWANN'07, IEEE-NANO'07, DCIS'07, GCoE'07, ARC'08, GCoE'08, ISCAS'08, ARC'09, NanoNet'09, IDT'10, IEEE-NANO'11, EDCC'12, IEEE-NANO'12, DTIS'13, ICECS'13 (3×), IIT'14, ICCCC'16, SOFA'16 (2×), ISREIE'16, ICCCC'18, ISREIE'18

208 Invitations

- 11 sessions/workshops, 18 plenary/keynote, 18 tutorials, 46 lectures, and 115 presentations

Reviewer

- USA National Science Foundation (8× since 2002), EU European Commission (6× since 2007), Belgium (2005, 2009), Cyprus (2009, 2010), Switzerland (2006, 2008), UAE (12×), Romania (14×)
- Journals: IEEE T. Nano., Nanotech., J. Nanotech., ACM JETC, IEEE T. VLSI, IEEE T. CAS, IEEE T. Design & Test, IEEE T. CAD, IEEE T. Comp., IEEE T. Sys. Man & Cyber., Microelectr., Integr. VLSI J., Electr. Lett., J. VLSI, J. Circ. Th. & Appls., Solid State Electr., IEEE T. Neural Nets, Neural Nets., Neural Net. World, Neural Proc. Lett., Intl. J. Neural Syst., Microelectr. J., New J. Phys., Biol. Cyber.
- Conferences (besides those organized): ADT'95, IJCNN'03, IIT'05, IWANN'05, IIT'06, ISCAS'06, ICSPC'07, ISIE-07, ISCAS'07, VTS'07, IECON'08, ISCAS'08, IJCNN'08, IECON'09, ICMLA'09, IIT'09, ISIE'10, ISSCI'10, MWSCAS'10, Optim'10, ECCTD'11, IEEE-NANO'11, IIT'11, IJCNN'11, MoNaCom'11, ESANN'12, IDT'12, IIT'12, IJCNN'12, DTIS'13, ADVCIT'14, I4CT'14, IJCNN'14, ISCAS'15, WSC'15, MWSCAS'17, SoCPar'17, MWSCAS'18
- Intl. Assoc. Sci. Tech. Develop. (IASTED), Intl. Soc. Mini & Microcomp. (ISMM), Intl. Comp. Sci. Conventions (ICSC), Natl. Info. & Documentation Inst. (INID)
- Books (5), PhD theses (13), MSc theses (6)

RESEARCH PLANS

"Success … going from failure to failure with undiminished enthusiasm." Winston Churchill

SHORT TO MEDIUM TERM

- *Atto-Joule designs based on a novel enabling reliability-optimal sizing of arrays of transistors*
- *Practical (economical) fault-tolerant communication and computations (from devices and wires)*
- *Designing in the reliability-power-delay realm for CMOS and beyond (SET, NEMS, molecular, hybrids)*

LONG TERM

- ***Bio-/brain-inspired nano-circuits/architectures for innovative information processing***

BIO-INSPIRED NANO-CIRCUIT ARCHITECTURES

– Designing innovative adaptive bio-/brain-inspired VLSI circuits and nano-architectures, allowing for low-power (near-threshold, mixed digital/analog, SET, molecular, and hybrids) and fault-tolerant (novel device-level redundancy schemes) large scale array-based information processing systems.

HIGH LEVEL AUTOMATIC SYNTHESIS

– Biological computing blocks rely on a few bits, suggesting digit-wise computations in a base larger than two. Low-precision 'analog' blocks could be synthesized base on Kolmogorov's superposition. The outputs of 'analog' blocks should be combined by cyclic (i.e., with feedback) digital circuits. This could interface directly to analog inputs, and would merge memory with computations.

ACCURATE EDA ALGORITHMS FOR RELIABILITY

– Reliability calculations should start from devices and wires (not from gates), and modeling should include device variations, defects, and noises. GREDA (Gate Reliability EDA) was developed for very accurate gate reliability estimates. GREDA's results were taken to the system level by CR-EDA[2] (Circuit Reliability EDA for Evaluating Design Alternatives). Both tools are Bayesian-based and consider input vectors, device variations, and noises. Lately, noises on wires and non-Gaussian distributions have been investigated jointly with novel (patentable) statistical design concepts.

APPLICATIONS

SMART ASSOCIATIVE MEMORIES

– An interesting application is represented by smart/associative memory. A content addressable memory (CAM) is looking for an exact match. Typical examples include: the cache and the virtual page addressing (microprocessors), and the address lookup (Internet servers). A bio-inspired associative memory relies on best-match, returning one or more matches sorted by a given metric. Advantages: could deal with missing data and errors, could generalize, etc.

HIGH-PERF EN/DECRYPTION EN/DECODING

– The plan here is to evaluate solutions for ultra-fast en/decryption allowing for wire-speed implementation of public-key (e.g., RSA, ECC) and symmetric key (e.g., AES) cryptosystems. Algorithms for en/decoding (e.g., JPEG, MPEG, etc., based on FFT/DCT) should also be targeted.

AWARDS

"Results! … I know several thousand things that won't work." Thomas Edison

3 VISITING

2015	• Erasmus Mundus (Visiting Prof.)	European Union (TU Dresden/CfAED)	
2013	• Erasmus Mundus (Nano Scholar)	European Union (TU Dresden/CfAED)	
2005 – 2011	• Visiting Professor	Ulster University (UK)	

5 FELLOWSHIPS

1999 – 2001	• Rose Research Fellowship	Rose Research (USA)	0.1%
1996 – 1998	• Director's Postdoctoral Fellowship	Los Alamos National Laboratory (USA)	1.0%
1994 – 1996	• HCM Research Fellowship	European Union (King's College London, UK)	0.1%
1993 – 1994	• Research Fellowship	Concerted Research Action (Flemish Community)	
1991	• Fulbright Fellowship	Fulbright Commission (USA)	0.1%

2 SCHOLARSHIPS

1991 – 1993	• Doctoral Scholarship	Katholieke Universiteit Leuven (Belgium)	1.0%
1975 – 1980	• National Merit Scholarship	Ministry of Science & Education (Romania)	0.1%

Other recognitions

2018	• Best Paper Award	IEEE ICCCC'2018	2.0%
2016	• Excellence Award	UAV	1.0%
2009	• Research Affairs Recognition Award	UAEU	1.0%
2009	• Best Excellence in Scholarship Award	UAEU, College of IT	2.0%
2008	• Best Paper Award	UAEU Annual Research Conference	1.0%
2003	• Two Patents	US PTO (2)	
2002	• Six Patents	US PTO (3), Taiwan PTO (3)	
2001	• US resident under extraordinary ability	*"VLSI implementations of neural networks"*	
2001	• Two Patents	US PTO (2)	
2000	• Best Paper Award	IEEE CAS'2000	1.0%
1996	• Senior Member	IEEE	8.0%
1994	• PhD *summa cum laude*	Katholieke Universiteit Leuven (Belgium)	5.0%
1984	• One Patent	Romanian PTO (1)	
1980	• Best MSc Thesis Award	University "Politehnica" of Bucharest (Romania)	1.0%
1980	• Best Paper Awards (three times)	University "Politehnica" of Bucharest (Romania)	1.0%
1977	• Best Paper Awards (two times)	University "Politehnica" of Bucharest (Romania)	1.0%
1975	• Highest Award (at graduation)	National College of Informatics (Romania)	0.5%
1971 – 1975	• Gold Medal/First Prize (four times)	Romanian Physics Olympiad	0.1%

Additional information

Membership

1999	– Marie Curie Fellowship Association	MCFA
	– Association for Computing Machinery	ACM
1992	– *Senior Member* (since 1996) Institute of Electrical and Electronics Engineering	IEEE
	– International Neural Network Society	INNS
1991	– *Founding Member* European Neural Network Society	ENNS
	– Expert of the Romanian Academy of Science	
1979	– Lions Club International (Centre International de Rencontres Universitaire)	CIRU

Miscellaneous

2017 – 2018	MEN	CNATDCU (Ministry of Education Decree nr. 3991/06.06.2017)	Member
2013 – 2015	UAEU	Promotion Advisory Group	Member
2009 – 2015	UAEU	Mubadala Technology (previously ATIC) Advisory Board	Member
2013 – 2015	CIT	Promotion Committee	*Chair*
2005 – 2013	CIT	Promotion Committee (except 2007 – 2008)	Member
2014 – 2015	CIT	Peer Evaluation of Teaching (PET) Committee	Member
2010 – 2013	UAEU	Council (representing CIT)	Member
2008 – 2013	UAEU	Graduate Research Studies Board	Member
2008 – 2011	UAEU	Graduate Council	Member
2007 – 2009	UAEU	Technical Task Force (inspecting and receiving the new CIT building)	Member
2006 – 2010	UAEU	Research Affairs Committee	Member
2006 – 2007	UAEU	IT Receiving Committee	Member
2011 – 2013	CIT	Research Committee	Member
2011 – 2012	CIT	Graduate Program Committee	Member
2009 – 2011	CIT	Graduate Program Committee	*Chair*
2005 – 2011	CIT	Research & Graduate Studies Committee	*Chair*
2005 – 2008	CIT	Laboratories & Equipment Committee	*Chair*
2005 – 2006	CIT	Recruitment Committee	*Chair*

2006 – 2011	CIT Strategic Planning Committee	Member
2006 – 2010	CIT Recruitment Committee	Member
2006 – 2009	CIT Honors Committee	Member
2006 – 2007	CIT Academic Performance Assessment Committee	Member
2005 – 2011	CIT College Council	Member
2005 – 2008	CIT Curriculum Committee	Member

2006 –	• Established and leading *Nano-ART = Nano Architectural Research Team*
2009	External examiner for one PhD thesis (member of the examination committee)
2008	External examiner for four PhD theses (member of the examination committee)
2007	External examiner for one PhD thesis (member of the examination committee)
	External examiner HCT Men's College, Abu Dhabi (9 students, 4 projects)
2006	External examiner for one PhD thesis (member of the examination committee)
2005	External examiner for one PhD thesis (member of the examination committee)

2001 – 2005	• Member of the EECS Graduate Studies Committee	WSU
2001 – 2005	• Member of the Computer Engineering (Program) Committee	WSU
1998 – 2001	• International Computer Science Conventions/Academic Advisory Board	ICSC
1997 – 1998	• *Program Chairman* of the IEEE Los Alamos Section	LANL
1985 – 1990	• *Secretary* of the MSc Examination Board	UPB
1987 JULY	– *Chair* of the Students' National Computer Training Camp (Sinaia, Romania)	UPB
1985 – 1990	– *Chair* of the Students' Group for Scientific Computer Research	UPB

2011 – 2015	• *Associate Editor* IEEE Transactions on VLSI Systems	IEEE
2010 – 2015	• *Associate Editor* Nano Communication Networks	Elsevier
2009	• Emerging Technologies Group on Nanoscale Communications	IEEE
2005 – 2008	• *Associate Editor* IEEE Transactions on Neural Networks	IEEE
2005	• Task Force on Nano Architectures	IEEE-CS
2003	• Member of the Novel Nanoarchitectures Study Group CW4	SRC-NNI

2018 reviews	(ongoing)		2 Romania				13 journals	14 conferences
2017 reviews	–		3 Romania				5 journals	9 conferences
2016 reviews	–		9 Romania				2 journals	22 conferences
2015 reviews	–						8 journals	42 conferences
2014 reviews	– 1 NSF						30 journals	45 conferences
2013 reviews	– 1 NSF						31 journals	58 conferences
2012 reviews	–					2 MSc	33 journals	46 conferences
2011 reviews	– 7 NSF	2 EU					19 journals	31 conferences
2010 reviews	–	1 EU		1 Cyprus			14 journals	24 conferences
2009 reviews	–	1 EU	1 Belgium	1 Cyprus		1 PhD	13 journals	25 conferences
2008 reviews	– 8 NSF	1 EU	1 Switzerland			4 PhD	15 journals	33 conferences
2007 reviews	– 9 NSF	1 EU			1 book	1 PhD	9 journals	28 conferences
2006 reviews	– 1 NSF		1 Switzerland		2 books	1 PhD	15 journals	15 conferences
2005 reviews	– 1 NSF		1 Belgium		1 book	1 PhD	5 journals	11 conferences

[…]

PUBLICATIONS	273	36 INVITED AND 7 BEST PAPER AWARDS (BESIDES 46 OTHER CONFS. AND 67 TECH. REP.)		
CITED	1474	HAND COUNTED (EXCLUDING SELF-CITATIONS) – UPON REQUEST	PUBLICATIONS	H INDEX
~ 500	571/393	**Web of Science** (all/excluding self-citation all databases) http://www.researcherid.com/rid/F-7799-2015	144	11
~1100	1095	**Scopus** (all, i.e., including self-citations) http://www.scopus.com/authid/detail.url?authorId=7004865225	155	15
		http://orcid.org/0000-0001-8185-956X	176	
	1100	Semantic Scholar (all, i.e., including self-citations) https://www.semanticscholar.org/author/Valeriu-Beiu/9048129	94	36 HIC
~2400		**Google Scholar** (all, i.e., including self-citations)		
	2322	http://scholar.google.com/citations?user=u_PrdFwAAAAJ	277	23
	2509	Harzing Publish or Perish (all, i.e., including self-citations)	335	23

LINKS	FOUR INVITED PRESENTATIONS
2014	• Bio-Inspired Designing with Arrays CMOS Emerg. Tech. Res. CMOSETR'14, Grenoble, France, July 8, 2014 http://books.google.ca/books?id=OL3aAwAAQBAJ&pg=PA102
2013	• Why Biology Can and Silicon Can't TUDresden, Germany, July 11, 2013, http://nano.tu-dresden.de/pages/seminar_636.html http://nano.tu-dresden.de/pubs/slides_others/2013_07_11_Beiu.pdf
2010	• Trustworthy Wings of the Mysterious Butterflies Intl. Nanotech. Conf. INC6, Grenoble, France, May 19, 2010 (http://incnano.org/)
2010	• On Brain Inspired Nano Interconnects (tutorial) IEEE Intl. Joint Conf. Neural Nets. IJCNN'10, Barcelona, Spain, July 18, 2010 http://cis.ieee.org/cis-educational-repository/cis-video-archive.html https://ieeetv.ieee.org/player/embed_play/130009/videowidth https://ieeetv.ieee.org/player/embed_play/130008/videowidth

LINKS	RELATED TO VITA	
1971 – 1975	• "Tudor Vianu" National College of Informatics	http://www.lbi.ro/
1975 – 1980	• University "Politehnica" of Bucharest Faculty of Control & Computers CS&E Department MSc supervisor	http://www.upb.ro/en/ http://acs.pub.ro/en/ https://cs.pub.ro/ http://ro.wikipedia.org/wiki/Mircea_Petrescu
1980 – 1982	• Research Institute for Computer Techniques	http://www.itc.ro/
1982 – 2001	• University "Politehnica" of Bucharest Faculty of Control & Computers CS&E Department	http://www.upb.ro/en/ http://acs.pub.ro/en/ https://cs.pub.ro/
1991 – 1994	• Katholieke Universiteit Leuven Faculty of Engineering EE Department (ESAT) PhD supervisor	http://www.kuleuven.be/english http://eng.kuleuven.be/en http://www.esat.kuleuven.be/en http://www.esat.kuleuven.be/stadius/person.php?id=18
1994 – 1996	• EU HCM Fellowship	Archived http://collections.internetmemory.org/haeu/20160826184856/http://cordis.europa.eu/tmr/src/grants/chbi/chbig_ro.htm
	• King's College London School of Natural & Mathematical Sciences Department of Mathematics Centre for Neural Networks Scientific advisor	http://www.kcl.ac.uk/ http://www.kcl.ac.uk/nms/ http://www.kcl.ac.uk/nms/depts/mathematics/ http://www.mth.kcl.ac.uk/cnn/ [old link; not active] http://en.wikipedia.org/wiki/John_G._Taylor
1996 – 1998	• Los Alamos National Laboratory Nonproliferation & International Security	http://www.lanl.gov/ http://nis-www.lanl.gov/ [old link; changed]
1998 – 2001	• RN2R/Rose Research LLC	http://patents.justia.com/assignee/RN2RLLC.html
2001 – 2005	• Washington State University School of EE&CS	http://www.wsu.edu/ http://school.eecs.wsu.edu/
2005 – 2011	• University of Ulster Intelligent System Research Centre	http://www.ulster.ac.uk/ Updated (several times) https://www.ulster.ac.uk/research/institutes/computer-science/groups/intelligent-systems-research-centre
2005 –	• United Arab Emirates University College of Information Technology	http://www.uaeu.ac.ae/en/ http://www.cit.uaeu.ac.ae/en/
2015 –	• "Aurel Vlaicu" University of Arad	http://www.uav.ro/en/