

1. ISI		JOURNAL ARTICLES (NUMBERING IS INVERSE CHRONOLOGICAL)	
J ₃₉	S.R. Cowell, S. Hoara, and V. Beiu Approximating Hammocks' Reliability with Beta Distributions Intl. J. Computers Communication & Control (IF ~ 2.093, SJR ~ 0.401)		Accepted
J ₃₈	V. Beiu: Brain Inspired Nano Architectures Intl. J. Computers Communication & Control (IF ~ 2.093, SJR ~ 0.401)	Invited	Accepted
J ₃₅	V. Dragoi, and V. Beiu Studying the Binary Erasure Polarization Subchannels Using Network Reliability IEEE Comm. Lett., vol. 24, no. 1, Jan. 2020 (IF ~ 3.419, SJR ~ 1.261) https://doi.org/10.1109/LCOMM.2019.2947910 WOS:000508630200014		62–66
J ₃₄	V. Dragoi, S.R. Cowell, V. Beiu, S. Hoara, and P. Gaşpar How Reliable Are Compositions of Series and Parallel Networks Compared with Hammocks? Intl. J. Comp. Comm. & Ctrl., vol. 13, no. 5, Oct. 2018 (IF = 1.585, SJR ~ 0.368) https://doi.org/10.15837/ijccc.2018.5.3354 WOS:000445916200002		772–791
J ₃₃	M. Tache, W. Ibrahim, F. Kharbash, and V. Beiu Reliability and Performance of Optimised Schmitt Trigger Gates IET Journal of Engineering, vol. 2018, no. 8, Aug. 2018 https://doi.org/10.1049/joe.2018.0091 WOS:000444338700004		735–744
J ₃₁	S.R. Cowell, V. Beiu, L. Dauş, and P. Poulin On the Exact Reliability Enhancements of Small Hammock Networks IEEE Access, vol. 6, no. 1, Apr. 2018 (IF = 4.098, SJR = 0.609) https://doi.org/10.1109/ACCESS.2018.2828036 WOS:000433619800001		25411–25426
J ₃₀	R.-M. Beiu, V. Beiu and V.-F. Duma Fiber Optic Mechanical Deformation Sensors Employing Perpendicular Photonic Crystals Optics Express, vol. 25, no. 19, 18 Sept. 2017 (IF = 3.561, SJR = 1.473) https://doi.org/10.1364/OE.25.023388 WOS:000411584600108		23388–23398
J ₂₈	V. Beiu, and L. Dauş Reliability Bounds for Two Dimensional Consecutive Systems Nano Communication Networks, vol. 6, no. 3, Sept. 2015 (SJR = 0.469) Special Issue on Biological Information and Communication Technology https://doi.org/10.1016/j.nancom.2015.04.003 WOS:000374412900008	Invited	145–152
J ₂₇	L. Dauş, and V. Beiu Lower and Upper Reliability Bounds for Consecutive- k -out-of- $n:F$ Systems IEEE Transactions on Reliability, vol. 64, no. 3, Sept. 2015 (IF = 2.287, SJR = 1.930) https://doi.org/10.1109/TR.2015.2417527 WOS:000360794600026		1128–1135
J ₂₆	M. Tache, V. Beiu, W. Ibrahim, F. Kharbash, and M. Alioto Enhancing the Static Noise Margins by Sizing Length for Ultra-Low Voltage/Power/Energy Gates Journal of Low Power Electronics, vol. 10, no. 1, Mar. 2014 (SJR = 0.186) https://doi.org/10.1166/jolpe.2014.1305 ISI ESCI	Invited	137–148

- J₂₅ G. Wendin, D. Vuillaume, M. Calame, S. Yitzchaik, C. Gamrat, G. Cuniberti, and V. Beiu
 SYMONE Project: SYnaptic MOlecular NETworks for Bio-inspired Information Processing
 Journal of Unconventional Computing, vol. 8, no. 4, Nov. 2012 (IF = 0.431, SJR = 0.205) 325–332
<http://www.oldcitypublishing.com/journals/ijuc-home/ijuc-issue-contents/ijuc-volume-8-number-4-2012/ijuc-8-4-p-325-332/>
 WOS:000312177000008
- J₂₄ W. Ibrahim, V. Beiu, and A. Beg
 Optimum Reliability Sizing for Complementary Metal Oxide Semiconductor Gates
 IEEE Transactions on Reliability, vol. 61, no. 3, Sept. 2012 (IF = 2.293, SJR = 1.516) 675–686
<https://doi.org/10.1109/TR.2012.2206249>
 WOS:000308424000006
- J₂₃ W. Ibrahim, V. Beiu, and A. Beg
 GREDA: A Fast and More Accurate CMOS Gates Reliability EDA Tool
 IEEE Transactions on Computer-Aided Design of Integrated Circuits & Systems
 vol. 31, no. 4, Apr. 2012 (IF = 1.093, SJR = 0.790) 509–521
<https://doi.org/10.1109/TCAD.2011.2176123>
 WOS:000302177200005
- J₂₂ W. Ibrahim, and V. Beiu
 Using Bayesian Networks to Accurately Calculate the Reliability of CMOS Gates
 IEEE Transactions on Reliability, vol. 60, no. 3, Sept. 2011 (IF = 1.285, SJR = 1.337) 538–549
<https://doi.org/10.1109/TR.2011.2161032>
 WOS:000294543800003
- J₂₁ V. Beiu, and W. Ibrahim
 Devices and Input Vectors Are Shaping von Neumann Multiplexing
 IEEE Transactions on Nanotechnology, vol. 10, no. 3, May 2011 (IF = 2.292, SJR = 1.271) 606–616
<https://doi.org/10.1109/TNANO.2010.2059036>
 WOS:000292963500036
- J₁₉ W. Ibrahim, and V. Beiu: Threshold Voltage Variations Make Full Adders Reliabilities Similar
 IEEE Transactions on Nanotechnology, vol. 9, no. 6, Nov. 2010 (IF = 1.864, SJR = 1.203) 664–667
<https://doi.org/10.1109/TNANO.2010.2066573>
 WOS:000284091300002
- J₁₈ W. Ibrahim, V. Beiu, and M.H. Sulieman: On the Reliability of Majority Gates Full Adders
 IEEE Transactions on Nanotechnology, vol. 7, no. 1, Jan. 2008 (IF = 2.154, SJR = 1.387) 56–67
<https://doi.org/10.1109/TNANO.2007.915203>
 WOS:000252518300010
- J₁₇ V. Beiu, S. Aunet, J. Nyathi, R.R. Rydberg III, and W. Ibrahim
 Serial Addition: Locally Connected Architectures
 IEEE Transactions on Circuits & Systems I, vol. 54, no. 11, Nov. 2007 (IF = 1.204, SJR = 1.438)
 Special Issue on Circuits and Computing Architectures for Nanotechnology 2564–2579
<https://doi.org/10.1109/TCSI.2007.907885>
 WOS:000250992900023
- J₁₆ M.H. Sulieman, and V. Beiu: On Single Electron Technology Full Adders
 IEEE Transactions on Nanotechnology, vol. 4, no. 6, Nov. 2005 (IF = 2.112, SJR = 2.455) 669–680
<https://doi.org/10.1109/TNANO.2005.858609>
 WOS:000233341100004
- J₁₅ S. Roy, and V. Beiu
 Majority Multiplexing — Economical Redundant Fault-Tolerant Design for Nano Architectures
 IEEE Transactions on Nanotechnology, vol. 4, no. 4, Jul. 2005 (IF = 2.112, SJR = 2.455) 441–451
<https://doi.org/10.1109/TNANO.2005.851251>
 WOS:000230421100009
- J₁₄ V. Beiu, J.M. Quintana, and M.J. Avedillo
 VLSI Implementations of Threshold Gates — A Comprehensive Survey
 IEEE Transactions on Neural Networks, vol. 14, no. 5, May 2003 (IF = 1.666, SJR = 1.727)
 Special Issue on Hardware Implementations of Neural Networks 1217–1243
<https://doi.org/10.1109/TNN.2003.816365>
 WOS:000186478900022
- J₁₁ V. Beiu, S. Draghici, and T. De Pauw

A Constructive Approach to Calculating Lower Entropy Bounds
 Neural Processing Letters, vol. 9, no. 1, Feb. 1999 (IF = 0.405, SJR = 1.162) 1–12
<https://doi.org/10.1023/A:1018659009494> WOS:000078809200001

J₁₀ V. Beiu, and H.E. Makaruk: Deeper Sparsely Nets Can Be Optimal
 Neural Processing Letters, vol. 8, no. 3, Dec. 1998 (IF = 0.286, SJR later) 201–210
<https://doi.org/10.1023/A:1009665432594> WOS:000077408700001

J₉ V. Beiu: On the Circuit and VLSI Complexity of Threshold Gate COMPARISON
 Neurocomputing, vol. 19, no. 1, Apr. 1998 (IF = 0.453, SJR later) 77–98
[https://doi.org/10.1016/S0925-2312\(97\)00099-4](https://doi.org/10.1016/S0925-2312(97)00099-4) WOS:000073365000008

J₇ V. Beiu, and J.G. Taylor
 On the Circuit Complexity of Sigmoid Feedforward Neural Networks
 Neural Networks, vol. 9, no. 7, Oct. 1996 (IF = 1.325, SJR later) 1155–1171
[https://doi.org/10.1016/0893-6080\(96\)00130-X](https://doi.org/10.1016/0893-6080(96)00130-X) WOS:A1996VQ82800006

Remark: The following 5 patents are indexed in ISI WoS (under Derwent Innovations Index)

P₁₁ V. Beiu: Low-Power Differential Conductance-Based Logic Gate and Method of Operation Thereof
 US 6,580,296, June 17, 2003 1–18
<https://patents.google.com/patent/US6580296/> DIIDW:2003656312

P₁₀ V. Beiu: Microprocessor and a Digital Signal Processor Including Adder and Multiplier Circuits
 Employing Logic Gates Having Discrete and Weighted Inputs
 US 6,516,331, February 4, 2003 1–14
<https://patents.google.com/patent/US6516331/> DIIDW:2000349800

P₈ V. Beiu: Adder Having Reduced Number of Internal Layers and Method of Operation Thereof
 US 6,438,572, August 20, 2002 [Also as WO/2001/023992 and AU40251/01] 1–11
<https://patents.google.com/patent/US6438572/> DIIDW:2001316145

P₇ V. Beiu: Noise Tolerant Conductance-Based Logic Gate and Methods of Operation and
 Manufacturing Thereof
 US 6,430,585, August 6, 2002 [Also as WO/2001/024367 and AU76009/00] 1–16
<https://patents.google.com/patent/US6430585/> DIIDW:2001281699

P₃ V. Beiu: Logic Gate Having Reduced Power Dissipation and Method of Operation Thereof
 US 6,259,275, July 10, 2001 1–19
<https://patents.google.com/patent/US6259275/> DIIDW:2001595137

2. ISI PROCEEDINGS ARTICLES (NUMBERING IS INVERSE CHRONOLOGICAL)

C₂₁₂ M. Nagy, V. Dragoi, and V. Beiu
 Employing Sorting Nets for Designing Reliable Computing Nets
 IEEE International Conference on Nanotechnology IEEE-NANO 2020
 Virtual conference [Montreal, QC, Canada], July 29-31, 2020 370–375
<https://doi.org/10.1109/NANO47656.2020.9183395> WOS:Pending

C₂₁₁ S.R. Cowell, S. Hoara, and V. Beiu
 Experimenting with Beta Distributions for Approximating Hammocks' Reliability
 International Conference on Computers Communications and Control ICCCG2020
 Virtual conference [Oradea, Romania], May 11-15, 2020 **Best Paper Award_s**
 In I. Dzitac et al. (Eds.): ICCCG 2020, SpringerNature, AISC 1243, 2021 70–81
https://doi.org/10.1007/978-3-030-53651-0_6 WOS:Pending

C₂₁₀ S. Hoara, R.-M. Beiu, and V. Beiu
 Investigating Hammock Networks on IBM Q

- International Conference on Computers Communications and Control ICCCC2020
Virtual conference [Oradea, Romania], May 11-15, 2020
In I. Dzitac et al. (Eds.): ICCCC 2020, SpringerNature, AISC 1243, 2021 57–69
https://doi.org/10.1007/978-3-030-53651-0_5 WOS:Pending
- C₂₀₉ S.R. Cowell, M. Nagy, and V. Beiu
Reliability of Two-Terminal Networks Equivalent to Small Optimal Sorting Nets
International Conference on Computers Communications and Control ICCCC2020
Virtual conference [Oradea, Romania], May 11-15, 2020
In I. Dzitac et al. (Eds.): ICCCC 2020, SpringerNature, AISC 1243, 2021 45–56
https://doi.org/10.1007/978-3-030-53651-0_4 WOS:Pending
- C₂₀₈ V. Dragoi, S.R. Cowell, and V. Beiu
Tight Bounds on the Coefficients of Consecutive k -out-of- $n:F$ Systems
International Conference on Computers Communications and Control ICCCC2020
Virtual conference [Oradea, Romania], May 11-15, 2020
In I. Dzitac et al. (Eds.): ICCCC 2020, SpringerNature, AISC 1243, 2021 35–44
https://doi.org/10.1007/978-3-030-53651-0_3 WOS:Pending
- C₂₀₆ V. Beiu, S.R. Cowell, and V. Dragoi
The Posets for Reliability: How Fine Can They Be?
International Workshop on Soft Computing Applications SOFA'18
Arad, Romania, September 13-15, 2018
In V.E. Balas et al. (Eds.): SOFA 2018, SpringerNature, AISC 1221, 2021 115–129
https://doi.org/10.1007/978-3-030-51992-6_10 WOS:Pending
- C₂₀₅ V. Dragoi, S.R. Cowell, and V. Beiu
Ordering Series and Parallel Compositions
IEEE International Conference on Nanotechnology IEEE-NANO'18
Cork, Ireland, July 23-26, 2018 8626408(1–4)
<https://doi.org/10.1109/NANO.2018.8626408> WOS:000458785600186
- C₂₀₄ S.R. Cowell, V. Dragoi, N.-C. Rohatinovici, and V. Beiu
Effective Conductances of Moore-Shannon Hammocks
IEEE International Conference on Nanotechnology IEEE-NANO'18
Cork, Ireland, July 23-26, 2018 8626295(1–4)
<https://doi.org/10.1109/NANO.2018.8626295> WOS:000458785600076
- C₂₀₂ R.-M. Beiu, V.-F. Duma, and V. Beiu
The Latest on the Axon Initial Segment
IEEE International Conference on Computers Communications and Control ICCCC'18
Baile Felix/Oradea, Romania, May 08-12, 2018 136–141
<https://doi.org/10.1109/ICCC.2018.8390450> WOS:000437157500021
- C₂₀₁ N.-C. Rohatinovici, S.R. Cowell, L. Daus, P. Poulin, V. Dragoi, V.E. Balaş, and V. Beiu
On Algorithms for Evaluating the Reliability of Large Hammock Networks
IEEE International Conference on Computers Communications and Control ICCCC'18
Baile Felix/Oradea, Romania, May 08-12, 2018 131–135
<https://doi.org/10.1109/ICCC.2018.8390449> WOS:000437157500020
- C₂₀₀ V. Dragoi, S.R. Cowell, S. Hoara, P. Gaşpar, and V. Beiu
Can Series and Parallel Compositions Improve on Hammocks? **Best Paper Award**, 124–130
IEEE International Conference on Computers Communications and Control ICCCC'18
Baile Felix/Oradea, Romania, May 08-12, 2018
<https://doi.org/10.1109/ICCC.2018.8390448> WOS:000437157500019
- C₁₉₉ V. Beiu, S.R. Cowell, V. Dragoi, S. Hoara, and P. Gaşpar

- Hammocks versus Hammock
IEEE International Conference on Computers Communications and Control ICCCC'18
Baile Felix/Oradea, Romania, May 08-12, 2018 119–123
<https://doi.org/10.1109/ICCCC.2018.8390447> WOS:000437157500018
- C₁₉₈ M. Nagy, S.R. Cowell, and V. Beiu
Are 3D Fibonacci Spirals for Real ? — From Science to Arts and Back to Science
IEEE International Conference on Computers Communications and Control ICCCC'18
Baile Felix/Oradea, Romania, May 08-12, 2018 91–96
<https://doi.org/10.1109/ICCCC.2018.8390443> WOS:000437157500014
- C₁₉₇ R.-M. Beiu, V. Beiu, and V.-F. Duma: Ultra-small Mechanical Deformation Sensor
Using a Hybrid Fiber Optic-based Triangular Photonic Crystal Structure
SPIE Photonics Europe 2018 (SPIE Vol. 10678)
Strasbourg, France, April 22-26, 2018 106780Z(1–6)
<https://doi.org/10.1117/12.2307017> WOS:000453085900025
- C₁₉₆ S.R. Cowell, V. Beiu, L. Daus, and P. Poulin
On Cylindrical Hammock Networks
IEEE International Conference on Nanotechnology IEEE-NANO'17
Pittsburgh, USA, July 25-28, 2017 185–188
<https://doi.org/10.1109/NANO.2017.8117498> WOS:000434647500042
- C₁₉₅ R.-M. Beiu, V.-F. Duma, and V. Beiu
Transverse 2D Photonic Crystal Inside a Fiber Optic for Picometer-scale Measurements
IEEE International Conference on Numerical Simulation of Optoelectronic Devices NOSUD'17
Copenhagen, Denmark, July 24-28, 2017 53–54
<https://doi.org/10.1109/NUSOD.2017.8009987> WOS:000426853800027
- C₁₉₄ V. Beiu: Photonic Techniques for Brain Imaging *Invited₂₇*
SPIE-SRLS International Conference for Lasers in Medicine ICLM'17
Timisoara, Romania, July 13-15, 2017 108310I(1–4)
<https://doi.org/10.1117/12.2282763> WOS:000453614200013
- C₁₉₃ R.-M. Beiu, V. Beiu, and V.-F. Duma
Fundamentals and biomedical applications of photonic crystals: An overview
SPIE-SRLS International Conference for Lasers in Medicine ICLM'17
Timisoara, Romania, July 13-15, 2017 108310R(1–5)
<https://doi.org/10.1117/12.2282019> WOS:000453614200022
- C₁₉₂ V. Beiu, L. Daus, N.C. Rohatinovici, and V.E. Balas
Transport Reliability on Axonal Cytoskeleton
IEEE International Conference on Engineering of Modern Electric Systems EMES'17
Oradea, Romania, June 1-2, 2017 160–163
<https://doi.org/10.1109/EMES.2017.7980404> WOS:000427085200037
- C₁₉₁ S.R. Cowell, V. Beiu, L. Daus, and P. Poulin
On Hammock Networks – Sixty Years After
IEEE International Conference on Design & Technology of Integrated Systems in
Nanoscale Era DTIS'17, Palma de Mallorca, Spain, April 4-6, 2017 792987I(1–6)
<https://doi.org/10.1109/DTIS.2017.7929871> WOS:000403402000002
- C₁₉₀ R. Todorean (Aldea), O. Geman, I. Chiuchisan, V.E. Balas, and V. Beiu
Novel Method for Neurodegenerative Disorders Screening Patients using
Hurst Coefficients on EEG Delta Rhythm
IEEE International Workshop on Soft Computing Applications SOFA'16
Arad, Romania, August 24-26, 2016

- In V.E. Balaş, L.C. Jain, and M.M. Balaş (eds.), *Soft Computing Applications*, Springer, 2018 349–358
https://doi.org/10.1007/978-3-319-62521-8_29 WOS:000433138300029
- C₁₈₉ V. Beiu, and M. Tache: Revisiting Delay Variations Statistically Through an Example
 IEEE International Semiconductor Conference CAS'15
 Sinaia, Romania, October 12-14, 2015 179–182
<https://doi.org/10.1109/SMICND.2015.7355200> WOS:000380566400034
- C₁₈₈ V. Beiu, and M. Tache: On Using Schmitt Trigger for Digital Logic
 IEEE International Semiconductor Conference CAS'15
 Sinaia, Romania, October 12-14, 2015 197–200
<https://doi.org/10.1109/SMICND.2015.7355206> WOS:000380566400038
- C₁₈₇ V. Beiu, and L. Dauş: Reliability Schemes for Nano-Communications
 IEEE European Conference on Circuit Theory and Design ECCTD'15
 Trondheim, Norway, August 24-26, 2015 7300038(1–4)
<https://doi.org/10.1109/ECCTD.2015.7300038> WOS:000380498200020
- C₁₈₆ V. Beiu, and M. Tache: Statistical Analysis of Static Noise Margins
 IEEE European Conference on Circuit Theory and Design ECCTD'15
 Trondheim, Norway, August 24-26, 2015 7300090(1–4)
<https://doi.org/10.1109/ECCTD.2015.7300090> WOS:000380498200072
- C₁₈₅ V. Beiu, and L. Dauş: On 2-Dimensional Consecutive Systems Once Again
 IEEE International Conference on Nanotechnology IEEE-NANO'15
 Rome, Italy, July 27-30, 2015 464–467
<https://doi.org/10.1109/NANO.2015.7388638> WOS:000380515200018
- C₁₈₄ V. Beiu, W. Ibrahim, M. Tache and F. Kharbash: When One Should Consider Schmitt Trigger Gates
 IEEE International Conference on Nanotechnology IEEE-NANO'15
 Rome, Italy, July 27-30, 2015 682–685
<https://doi.org/10.1109/NANO.2015.7388698> WOS:000380515200078
- C₁₈₃ M. Tache, V. Beiu, and T.-J. King Liu: Why Hybridize NEMS with CMOS?
 IEEE International Conference on Electronics Circuits and Systems ICECS'14
 Marseille, France, December 7-10, 2014 646–649
<https://doi.org/10.1109/ICECS.2014.7050068> WOS:000380548000163
- C₁₈₁ V. Beiu, and L. Dauş: Why Should We Care About Bounds – Consecutive Systems Revisited
 IEEE International Conference on Innovations in Information Technology IIT'14
 Al Ain, UAE, November 9-11, 2014 65–70
<https://doi.org/10.1109/INNOVATIONS.2014.6987563> WOS:000412231400012
- C₁₈₀ M. Tache, F. Kharbash, and V. Beiu: On SRAM Bit-Cells Once Again
 IEEE International Conference on Innovations in Information Technology IIT'14
 Al Ain, UAE, November 9-11, 2014 80–83
<https://doi.org/10.1109/INNOVATIONS.2014.6987566> WOS:000412231400015
- C₁₇₉ M. Tache, V. Beiu, and T.-J. King Liu: A Dual-Voltage Hybrid NEMS-CMOS Low Power Scheme
 IEEE International Semiconductor Conference CAS'14
 Sinaia, Romania, October 13-15, 2014 211–214
<https://doi.org/10.1109/SMICND.2014.6966438> WOS:000380488300042
- C₁₇₈ V. Beiu, M. Tache, and F. Kharbash: Reliability Enhanced SRAM Bit-Cells
 IEEE International Semiconductor Conference CAS'14
 Sinaia, Romania, October 13-15, 2014 229–232
<https://doi.org/10.1109/SMICND.2014.6966444> WOS:000380488300046
- C₁₇₇ V. Beiu, W. Ibrahim, M. Tache, and T.-J. King Liu: On Ultra-Low Power Hybrid NEMS-CMOS

- IEEE International Conference on Nanotechnology IEEE-NANO'14
Toronto, ON, Canada, August 18-21, 2014 201–206
<https://doi.org/10.1109/NANO.2014.6968045> WOS:000365620600046
- C₁₇₆ V. Beiu, and L. Daus: Review of Reliability Bounds for Consecutive- k -out-of- n Systems
IEEE International Conference on Nanotechnology IEEE-NANO'14
Toronto, ON, Canada, August 18-21, 2014 302–307
<https://doi.org/10.1109/NANO.2014.6968048> WOS:000365620600066
- C₁₇₅ M. Al Kaabi, A. Al Ali, H. Al Janahi, M. Al Kendi, M. Tache, and V. Beiu
Ultra-low Power SRAM Cells with Unconventional Sizing
IEEE International Conference on Nanotechnology IEEE-NANO'14
Toronto, ON, Canada, August 18-21, 2014 308–313
<https://doi.org/10.1109/NANO.2014.6968117> WOS:000365620600067
- C₁₇₄ F. Kharbash, V. Beiu, M. Tache, and W. Ibrahim
Using Body Bias when Upsizing Length for Maximizing the SNMs of CMOS Gates
IEEE International Conference on Electronics, Circuits, and Systems ICECS'13
Abu Dhabi, UAE, December 8-11, 2013 409–412
<https://doi.org/10.1109/ICECS.2013.6815441> WOS:000339725900111
- C₁₇₃ W. Ibrahim, V. Beiu, M. Tache, and F. Kharbash: On Schmitt Trigger and Other Inverters
IEEE International Conference on Electronics, Circuits, and Systems ICECS'13
Abu Dhabi, UAE, December 8-11, 2013 29–32
<https://doi.org/10.1109/ICECS.2013.6815337> WOS:000339725900008
- C₁₇₂ D. Arotaritei, V. Beiu, M. Turnea, and M. Rotariu
Probabilistic Gate Matrix for Axon-inspired Communication
IEEE International Conference on E-Health and Bioengineering EHB'13
Iasi, Romania, November 21-23, 2013 6707255(1–4)
<https://doi.org/10.1109/EHB.2013.6707255> WOS:000346672900023
- C₁₇₁ N.V. Acharya, J.L. Raju, A. Kumar, M. Tache, and V. Beiu: Monte Carlo Analysis of the
Static Noise Margins for CMOS Gates in Predictive Technology Models
IEEE GCC Conference and Exhibition, Doha, Qatar, November 17-20, 2013 5–10
<https://doi.org/10.1109/IEEEGCC.2013.6705739> WOS:000343832200002
- C₁₇₀ V. Beiu, M. Tache, W. Ibrahim, F. Kharbash, and M. Alioto
On Upsizing Length and Noise Margins
IEEE International Semiconductor Conference CAS'13
Sinaia, Romania, October 13-16, 2013 219–222
<https://doi.org/10.1109/SMICND.2013.6688659> WOS:000330180800043
- C₁₆₉ V. Beiu, A. Beg, W. Ibrahim, F. Kharbash, and M. Alioto
Enabling Sizing for Enhancing the Static Noise Margins
IEEE International Symposium on Quality in Electronic Design ISQED'13
Santa Clara, CA, USA, March 4-6, 2013 278–285
<https://doi.org/10.1109/ISQED.2013.6523623> WOS:000324653700042
- C₁₆₈ P. Santagati, and V Beiu: Will Thermal Noise Affect Nano-Communications?
IEEE International Conference on Communications, Signal Processing,
and their Applications ICCSPA'13, Sharjah, UAE, February 12-14, 2013 6487322(1–4)
<https://doi.org/10.1109/ICCSPA.2013.6487322> WOS:000318427600097
- C₁₆₆ V. Beiu, L. Iordaconiu, A. Beg, W. Ibrahim, and F. Kharbash
Low Power and Highly Reliable Gates Using Arrays of Optimally Sized Transistors
IEEE International Semiconductor Conference CAS'12

- Sinaia, Romania, October 15-17, 2012 433–436
<https://doi.org/10.1109/SMICND.2012.6400738> WOS:000314223700089
- C₁₆₅ A. Beg, V. Beiu, and W. Ibrahim
 Unconventional Transistor Sizing for Reducing Power Alleviates Threshold Voltage Variations
 IEEE International Semiconductor Conference CAS'12
 Sinaia, Romania, October 15-17, 2012 429–432
<https://doi.org/10.1109/SMICND.2012.6400739> WOS:000314223700088
- C₁₆₄ V. Beiu, M. Calame, G. Cuniberti, C. Gamrat, Z. Konkoli, D. Vuillaume, G. Wendin, and S. Yitzchaik
 Aspects of Computing with Locally Connected Networks
 AIP International Conference on Numerical Analysis and Applied Mathematics ICNAAM'12
 Kos, Greece, September 19-25, 2012 1875–1879
<https://doi.org/10.1063/1.4756547> WOS:000310698100443
- C₁₆₃ V. Beiu, A. Beg, W. Ibrahim, and F. Kharbash
 Towards Ultra-Low Voltage/Power Using Unconventionally Sized Arrays of Transistors
 IEEE International Conference on Nanotechnology IEEE-NANO'12
 Birmingham, UK, August 20-23, 2012 6322071(1–5)
<https://doi.org/10.1109/NANO.2012.6322071> WOS:000309933900186
- C₁₆₂ V. Beiu, W. Ibrahim, A. Beg, and M. Tache: On Axon-inspired Communications
 IEEE European Conference on Circuit Theory and Design ECCTD'11
 Linköping, Sweden, August 29-31, 2011 ECCTD'15 ... 789–792
<https://doi.org/10.1109/ECCTD.2011.6043841>
- C₁₆₁ V. Beiu, A. Beg, and W. Ibrahim: Atto-Joule Gates for the Whole Voltage Range *Invited*₂₅
 IEEE International Conference on Nanotechnology IEEE-NANO'11
 Portland, OR, USA, August 15-18, 2011 IEEE-NANO'09, '12 1424–1429
<https://doi.org/10.1109/NANO.2011.6144399>
- C₁₆₀ A. Beg, and V. Beiu: Ultra Low Power/Energy SET-based Axon-inspired Communication
 IEEE International Conference on Nanotechnology IEEE-NANO'11
 Portland, OR, USA, August 15-18, 2011 IEEE-NANO'09, '12 1183–1186
<https://doi.org/10.1109/NANO.2011.6144563>
- C₁₅₉ W. Ibrahim, A. Beg, and V. Beiu: Highly Reliable and Low-Power Full Adder Cell
 IEEE International Conference on Nanotechnology IEEE-NANO'11
 Portland, OR, USA, August 15-18, 2011 IEEE-NANO'09, '12 500–503
<https://doi.org/10.1109/NANO.2011.6144434>
- C₁₅₈ V. Beiu, L. Zhang, W. Ibrahim, and M. Tache
 Minimizing Communication Power Using Near-neighbor Axon-inspired Lattices
 IEEE International Conference on Nanotechnology IEEE-NANO'11
 Portland, OR, USA, August 15-18, 2011 IEEE-NANO'09, '12 426–430
<https://doi.org/10.1109/NANO.2011.6144502>
- C₁₅₇ J.J. Wade, L.J. McDaid, J. Harkin, V. Crunelli, J.A.S. Kelso, and V. Beiu
 Exploring Retrograde Signaling via Astrocytes as a Mechanism for Self Repair
 IEEE International Joint Conference on Neural Networks IJCNN'11
 San Jose, CA, USA, July 31 - August 5, 2011 3149–3155
<https://doi.org/10.1109/IJCNN.2011.6033638> WOS:000297541203042
- C₁₅₆ A. Beg, V. Beiu, and W. Ibrahim
 Atto Joule CMOS Gates Using Reversed Sizing and W/L Swapping
 IEEE International New Circuits and Systems Conference NEWCAS'11
 Bordeaux, France, June 26-29, 2011 NEWCAS'09 498–501

<https://doi.org/10.1109/NEWCAS.2011.5981328>

- C₁₅₅ W. Ibrahim, V. Beiu, and A. Beg: On NOR-2 von Neumann Multiplexing
IEEE International Design and Test Workshop IDT'10
Abu Dhabi, UAE, December 14-16, 2010 IDT'09 67–72
<https://doi.org/10.1109/IDT.2010.5724410>
- C₁₅₄ V. Beiu, and W. Ibrahim: From Transistor Variations to NAND-2 Multiplexing
IEEE International Conference on Nanotechnology IEEE-NANO'10
Seoul, Korea, August 17-20, 2010 IEEE-NANO'09, '12 1076–1081
<https://doi.org/10.1109/NANO.2010.5697864>
- C₁₅₃ W. Ibrahim, and V. Beiu: Device-Level Reliability of Several Full Adder Cells
IEEE International Conference on Nanotechnology IEEE-NANO'10
Seoul, Korea, August 17-20, 2010 IEEE-NANO'09,'12 1082–1087
<https://doi.org/10.1109/NANO.2010.5697865>
- C₁₅₂ M.H. Sulieman, V. Beiu, and W. Ibrahim
Low-Power and Highly Reliable Logic Gates: Transistor-level Optimizations
IEEE International Conference on Nanotechnology IEEE-NANO'10
Seoul, Korea, August 17-20, 2010 IEEE-NANO'09, '12 254–257
<https://doi.org/10.1109/NANO.2010.5697892>
- C₁₅₀ W. Ibrahim, and V. Beiu: Reliability of NAND-2 CMOS Gates from Threshold Voltage Variations
IEEE International Conference Innovations in Information Technology IIT'09
Al Ain, UAE, December 15-17, 2009 135–139
<https://doi.org/10.1109/IIT.2009.5413631> WOS:000283476800064
- C₁₄₉ V. Beiu, B.A.M. Madappuram, P.M. Kelly, and L.J. McDaid
On Two-layer Hierarchical Networks: How Does the Brain Do This? *Invited*₂₄
International ICST Conference on Nano-Networks Nano-Net'09
Luzern, Switzerland, October 18-20, 2009 231–241
https://doi.org/10.1007/978-3-642-04850-0_31 WOS:000301970000031
- C₁₄₈ P.M. Kelly, F. Tuffy, V. Beiu, and L.J. McDaid: Reduced Interconnects in Neural
Networks Using a Time Multiplexed Architecture Based on Quantum Devices *Invited*₂₃
International ICST Conference on Nano-Networks Nano-Net'09
Luzern, Switzerland, October 18-20, 2009 242–250
https://doi.org/10.1007/978-3-642-04850-0_32 WOS:000301970000032
- C₁₄₇ V. Beiu, W. Ibrahim, and R.Z. Makki: On Wires Holding a Handful of Electrons *Invited*₂₂
International ICST Conference on Nano-Networks Nano-Net'09
Luzern, Switzerland, October 18-20, 2009 259–269
https://doi.org/10.1007/978-3-642-04850-0_34 WOS:000301970000034
- C₁₄₆ W. Ibrahim, and V. Beiu: A Bayesian-based EDA Tool for Nano-Circuits Reliability Calculations *Invited*₂₁
International ICST Conference on Nano-Networks Nano-Net'09
Luzern, Switzerland, October 18-20, 2009 276–284
https://doi.org/10.1007/978-3-642-04850-0_36 WOS:000301970000036
- C₁₄₅ V. Beiu, B.A.M. Madappuram, P.M. Kelly, and L.J. McDaid
On Brain-inspired Hierarchical Network Topologies
IEEE International Conference on Nanotechnology IEEE-NANO'09
Genoa, Italy, July 26-30, 2009 202–205
<https://ieeexplore.ieee.org/document/5394594/> WOS:000302997400057
- C₁₄₄ W. Ibrahim, V. Beiu, and H. Amer
How Much Input Vectors Affect Nano-Circuit's Reliability Estimates

- IEEE International Conference on Nanotechnology IEEE-NANO'09
Genoa, Italy, July 26-30, 2009 699–702
<https://ieeexplore.ieee.org/document/5394482/> WOS:000302997400193
- C₁₄₃ V. Beiu, W. Ibrahim, and R.Z. Makki: On Wires at Low Electron Densities
IEEE International Conference on Nanotechnology IEEE-NANO'09
Genoa, Italy, July 26-30, 2009 703–706
<https://ieeexplore.ieee.org/document/5394862/> WOS:000302997400194
- C₁₄₁ W. Ibrahim, V. Beiu, and H. Amer: Why Should We Care About Input Vectors?
IEEE International Northeast Workshop on Circuit and Systems NEWCAS'09
Toulouse, France, June 28 - July 1, 2009 5290448(1–4)
<https://doi.org/10.1109/NEWCAS.2009.5290448> WOS:000275234500055
- C₁₄₀ V. Beiu, W. Ibrahim, and R.Z. Makki: On Wires Driven by a Few Electrons
IEEE International Northeast Workshop on Circuit and Systems NEWCAS'09
Toulouse, France, June 28 - July 1, 2009 5290455(1–4)
<https://doi.org/10.1109/NEWCAS.2009.5290455> WOS:000275234500092
- C₁₃₉ R.M. Beiu, and V. Beiu: Pico Sensors for All Seasons — When Light Performs Its Marvels
IEEE International Conference on Innovations in Information Technology IIT'08
Al Ain, UAE, December 16-18, 2008 116–120
<https://doi.org/10.1109/INNOVATIONS.2008.4781727> WOS:000274017600100
- C₁₃₈ R.M. Beiu, and V. Beiu
Fiber Optic Mechanical Sensor Based on a Triangular-lattice Photonic Crystal
IEEE International Photonics Global Conference IPGC'08
Singapore, December 8-11, 2008 4781347(1–4)
<https://doi.org/10.1109/IPGC.2008.4781347> WOS:000267591100050
- C₁₃₇ V. Beiu, B.A.M. Madappuram, and M. McGinnity
On Brain-inspired Hybrid Topologies for Nano-architectures — A Rent's Rule Approach
IEEE International Conference on Embedded Computer Systems IC-SAMOS'08
Samos, Greece, July 21-24, 2008 33–40
<https://doi.org/10.1109/ICSAMOS.2008.4664844> WOS:000262964400005
- C₁₃₄ B.A.M. Madappuram, V. Beiu, P.M. Kelly, and L.J. McDaid
On Brain-inspired Connectivity and Hybrid Network Topologies
IEEE/ACM International Symposium on Nanoscale Architectures NANOARCH'08
Anaheim, CA, USA, June 8-13, 2008 54–61
<https://doi.org/10.1109/NANOARCH.2008.4585792> WOS:000259442100008
- C₁₃₃ V. Beiu, and W. Ibrahim: Does the Brain Really Outperform Rent's Rule?
IEEE International Symposium on Circuits and Systems ISCAS'08
Seattle, WA, USA, May 18-21, 2008 640–643
<https://doi.org/10.1109/ISCAS.2008.4541499> WOS:000258532100163
- C₁₃₂ W. Ibrahim, V. Beiu, and S. Lazarova-Molnar: Accurate Nano-Circuits Reliability Evaluations
Based on Combining Numerical Simulations with Monte Carlo Ones
IEEE International Design and Test Workshop IDT'07
Cairo, Egypt, December 16-18, 2007 139–144
<https://doi.org/10.1109/IDT.2007.4437447> WOS:000252739600027
- C₁₃₁ S. Lazarova-Molnar, V. Beiu, and W. Ibrahim
Proxels for Reliability Assessment of Future Nano-Architectures
IEEE International Design and Test Workshop IDT'07
Cairo, Egypt, December 16-18, 2007 88–89

- <https://doi.org/10.1109/IDT.2007.4437435> WOS:000252739600018
- C₁₃₀ S. Lazarova-Molnar, V. Beiu, and W. Ibrahim
Reliability – The Fourth Optimization Pillar of Nanoelectronics
IEEE International Conference on Signal Processing and Communications ICSPC'07
Dubai, UAE, November 24-27, 2007 73–76
<https://doi.org/10.1109/ICSPC.2007.4728258> WOS:000266406700019
- C₁₂₉ W. Ibrahim, and V. Beiu: Why Nano-DSP Will Be Fan-in Constrained
IEEE International Conference on Signal Processing and Communications ICSPC'07
Dubai, UAE, November 24-27, 2007 317–320
<https://doi.org/10.1109/ICSPC.2007.4728319> WOS:000266406700080
- C₁₂₇ W. Ibrahim, V. Beiu, and Y.A. Alkhawwar: On the Reliability of Four Full Adder Cells
IEEE International Conference Innovations in Information Technology IIT'07
Dubai, UAE, November 18-20, 2007 720–724
<https://doi.org/10.1109/IIT.2007.4430508> WOS:000255983000146
- C₁₂₆ R.M. Beiu, C.D. Stanescu, and V. Beiu
A Novel Microstructured Fiber Optic Sensor for Very Small Deformations
SPIE International Symposium on Optomechatronic Technologies ISOT'07, SPIE vol. 6716
Lausanne, Switzerland, October 8-10, 2007 67160D(1–8)
<https://doi.org/10.1117/12.754190> WOS:000250821500012
- C₁₂₅ R.M. Beiu, C.D. Stanescu, and V. Beiu: Unique In-Fiber Photonic Crystal Sensor
IEEE International Midwest Symposium on Circuit and Systems MWSCAS'07
Montreal, Canada, August 5-8, 2007 116–119
<https://doi.org/10.1109/MWSCAS.2007.4488550> WOS:000257110900023
- C₁₂₄ R.M. Beiu, C.D. Stanescu, and V. Beiu: Highly Sensitive Nano-Photonic Embedded Sensors
IEEE International Conference on Nanotechnology IEEE-NANO'07
Hong Kong, China, August 2-5, 2007 737–741
<https://doi.org/10.1109/NANO.2007.4601293> WOS:000261434900166
- C₁₂₃ V. Beiu, W. Ibrahim, and S. Lazarova-Molnar
A Fresh Look at Majority Multiplexing – When Devices Get Into the Picture
IEEE International Conference on Nanotechnology IEEE-NANO'07
Hong Kong, China, August 2-5, 2007 883–888
<https://doi.org/10.1109/NANO.2007.4601325> WOS:000261434900198
- C₁₂₂ S. Lazarova-Molnar, V. Beiu, and W. Ibrahim
A Strategy for Reliability Assessment of Future Nano-Circuits
WSEAS International Conference on Circuits, Systems, Communications, Computers CSCC'07
Agios Nikolaos, Crete, Greece, July 23-28, 2007 60–65
<https://catalogue.nlg.gr/Record/b.523684/TOC> WOS:000249783300013
- C₁₂₁ W. Ibrahim, and V. Beiu: Long Live Small Fan-in Majority Gates – Their Reign Looks Like Coming!
IEEE International Conference on Application-specific Systems
Architectures and Processors ASAP'07, Montreal, Canada, July 8-11, 2007 278–283
<https://doi.org/10.1109/ASAP.2007.4429993> WOS:000255432100043
- C₁₂₀ V. Beiu, W. Ibrahim, and S. Lazarova-Molnar
What von Neumann Did Not Say About Multiplexing: Beyond Gates Failures – The Gory Details
International Work-Conference on Artificial Neural Networks IWANN'07
San Sebastián, Spain, June 19-22, 2007, Springer LNCS 4507 487–496
https://doi.org/10.1007/978-3-540-73007-1_60 WOS:000247839300060
- C₁₁₇ V. Beiu, W. Ibrahim, Y.A. Alkhawwar, and M.H. Sulieman

- Gate Failures Effectively Shape Multiplexing
IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems DFT'06
Washington, DC, USA, October 2-6, 2006 29–37
<https://doi.org/10.1109/DFT.2006.33> WOS:000242580800004
- C₁₁₆ V. Beiu, and M.H. Sulieman: On Practical Multiplexing Issues
IEEE International Conference on Nanotechnology IEEE-NANO'06
Cincinnati, OH, USA, July 16-20, 2006 IEEE-NANO'04, '07 310–313
<https://doi.org/10.1109/NANO.2006.247637>
- C₁₁₅ M.H. Sulieman, and V. Beiu: Multiplexing Schemes for Single Electron Technologies
IEEE International Conference on Computer Systems and Applications AICCSA'06
Sharjah, UAE, March 8-11, 2006 424–428
<https://doi.org/10.1109/AICCSA.2006.205125> WOS:000243337100066
- C₁₁₄ V. Beiu, J. Nyathi, S. Aunet, and M.H. Sulieman: Femto Joule Switching for Nano Electronics
IEEE International Conference on Computer Systems and Applications AICCSA'06
Sharjah, UAE, March 8-11, 2006 415–423
<https://doi.org/10.1109/AICCSA.2006.205124> WOS:000243337100065
- C₁₁₁ V. Beiu, and A. Zawadzki
On Kolmogorov's Superpositions: Novel Gates and Circuits for Nanoelectronics?
IEEE International Joint Conference on Neural Networks IJCNN'05
Montreal, Canada, July 31 - August 4, 2005 651–656
<https://doi.org/10.1109/IJCNN.2005.1555908> WOS:000235178000100
- C₁₁₀ S. Aunet, and V. Beiu: Ultra Low Power Fault Tolerant Neural Inspired CMOS Logic
IEEE International Joint Conference on Neural Networks IJCNN'05
Montreal, Canada, July 31 - August 4, 2005 2843–2848
<https://doi.org/10.1109/IJCNN.2005.1556376> WOS:000235178004032
- C₁₀₉ V. Beiu, S. Aunet, J. Nyathi, R. Rydberg III, and A. Djupdal
On the Advantages of Serial Architectures for Low-Power Reliable Computations
IEEE International Conference on Application-specific Systems,
Architectures and Processors ASAP'05, Samos, Greece, July 23-25, 2005 276–281
<https://doi.org/10.1109/ASAP.2005.48> WOS:000231660100040
- C₁₀₈ V. Beiu, A. Djupdal, and S. Aunet
Ultra Low-Power Neural Inspired Addition – When Serial Might Outperform Parallel Architectures
International Work-Conference on Artificial Neural Networks IWANN'05
Barcelona, Spain, June 8-10, 2005, Springer LNCS 3512 486–493
https://doi.org/10.1007/11494669_60 WOS:000230384000060
- C₁₀₇ V. Beiu, A. Zawadzki, R. Andonie, and S. Aunet
Using Kolmogorov Inspired Gates for Low Power Nanoelectronics
International Work-Conference on Artificial Neural Networks IWANN'05
Barcelona, Spain, June 8-10, 2005, Springer LNCS 3512 438–445
https://doi.org/10.1007/11494669_54 WOS:000230384000054
- C₁₀₆ V. Beiu: A Novel Highly Reliable Low-Power Nano Architecture
When von Neumann Augments Kolmogorov *Invited*₁₆
IEEE International Conference on Application-specific Systems
Architectures and Processors ASAP'04, Galveston, TX, USA, September 27-29, 2004 167–177
<https://doi.org/10.1109/ASAP.2004.1342467> WOS:000224568700014
- C₁₀₅ V. Beiu, U. Rückert, S. Roy, and J. Nyathi
On Nanoelectronic Architectural Challenges and Solutions

- IEEE International Conference on Nanotechnology IEEE-NANO'04
Munich, Germany, August 17-19, 2004 628–631
<https://doi.org/10.1109/NANO.2004.1392441> WOS:000226085100209
- C₁₀₄ M.H. Sulieman, and V. Beiu: On Single Electron Technology Full Adders
IEEE International Conference on Nanotechnology IEEE-NANO'04
Munich, Germany, August 17-19, 2004 317–320
<https://doi.org/10.1109/NANO.2004.1392337> WOS:000226085100106
- C₁₀₃ S. Roy, and V. Beiu: Multiplexing Schemes for Cost-Effective Fault-Tolerance
IEEE International Conference on Nanotechnology IEEE-NANO'04
Munich, Germany, August 17-19, 2004 589–592
<https://doi.org/10.1109/NANO.2004.1392429> WOS:000226085100197
- C₁₀₂ M.H. Sulieman, and V. Beiu
Design and Analysis of SET Circuits – Using MATLAB Modules and Simon
IEEE International Conference on Nanotechnology IEEE-NANO'04
Munich, Germany, August 17-19, 2004 618–621
<https://doi.org/10.1109/NANO.2004.1392438> WOS:000226085100206
- C₁₀₁ J. Nyathi, V. Beiu, S. Tatapudi, and D.J. Betowski
A Charge Recycling Differential Noise-Immune Perceptron
IEEE International Joint Conference on Neural Networks IJCNN'04
Budapest, Hungary, July 25-29, 2004 1995–2000
<http://doi.org/10.1109/IJCNN.2004.1380921> WOS:000224941900345
- C₁₀₀ D.J. Betowski, D. Dwyer, and V. Beiu
A Novel Segmented Parabolic Sine Approximation for Direct Digital Frequency Synthesizers
International Multi-conference VLSI'04, Las Vegas, NV, USA, June 21-25, 2004 523–529
<https://dblp.uni-trier.de/db/conf/csreaESA/csreaESA2004.html> WOS:000225884700077
- C₉₉ V. Beiu, and M.H. Sulieman
Optimal Practical Perceptron Addition – Application to Single Electron Technology
International Multi-conference VLSI'04, Las Vegas, NV, USA, June 21-25, 2004 541–547
<https://dblp.uni-trier.de/db/conf/csreaESA/csreaESA2004.html> WOS:000225884700080
- C₉₈ M.H. Sulieman, and V. Beiu
Characterization of a 16-bit Threshold Logic Single Electron Technology Adder
IEEE International Symposium on Circuits and Systems ISCAS'04
Vancouver, Canada, May 23-26, 2004 681–684
<https://doi.org/10.1109/ISCAS.2004.1328838> WOS:000223102200171
- C₉₇ M.H. Sulieman, and V. Beiu: On the Design of Multibit SET Adders
NSTI Nanotechnology NanoTech'04, Boston, MA, USA, March 7-11, 2004, vol. 3 169–172
<https://www.nsti.org/Nanotech2004/showabstract.html?absno=226> WOS:000223078200046
- C₉₆ V. Beiu: Threshold Logic Implementations – The Early Days
IEEE International Midwest Symposium on Circuit and Systems MWSCAS'03
Cairo, Egypt, December 27-30, 2003 1379–1383
<https://doi.org/10.1109/MWSCAS.2003.1562552> WOS:000234964300337
- C₉₅ V. Beiu, D.J. Betowski, and P.-S. Wu
Over 100 dBc ROM-less Piecewise Non-linear Direct Digital Frequency Synthesizers
IEEE International Midwest Symposium on Circuit and Systems MWSCAS'03
Cairo, Egypt, December 27-30, 2003 760–763
<https://doi.org/10.1109/MWSCAS.2003.1562397> WOS:000234964300188
- C₉₄ V. Beiu, J.M. Quintana, M.J. Avedillo, and M.H. Sulieman

- Threshold Logic – From Vacuum Tubes to Nanoelectronics *Invited*₁₅
 IEEE International Midwest Symposium on Circuit and Systems MWSCAS'03
 Cairo, Egypt, December 27-30, 2003 930–935
<https://doi.org/10.1109/MWSCAS.2003.1562439> WOS:000234964300230
- C₉₃ M.H. Sulieman, and V. Beiu *Invited*₁₄
 Review of Recent Full Adders Implemented in Single Electron Technology
 IEEE International Midwest Symposium on Circuit and Systems MWSCAS'03
 Cairo, Egypt, December 27-30, 2003 872–875
<https://doi.org/10.1109/MWSCAS.2003.1562425> WOS:000234964300216
- C₉₂ P.-S. Wu, and V. Beiu
 On Accurate Piecewise Linear ROM-less Direct Digital Frequency Synthesizers
 IEEE International Conference on Neural Networks and Signal Processing ICNNSP'03
 Nanjing, China, December 14-17, 2003 1595–1599
<https://doi.org/10.1109/ICNNSP.2003.1281185> WOS:000189460400387
- C₉₁ M.H. Sulieman, and V. Beiu: Optimal Practical Adders Using Perceptrons
 IEEE International Conference on Neural Networks and Signal Processing ICNNSP'03
 Nanjing, China, December 14-17, 2003 345–348
<https://doi.org/10.1109/ICNNSP.2003.1279280> WOS:000189460400082
- C₉₀ D.J. Betowski, and V. Beiu
 Considerations for Phase Accumulator Design for Direct Digital Frequency Synthesizers
 IEEE International Conference on Neural Networks and Signal Processing ICNNSP'03
 Nanjing, China, December 14-17, 2003 176–179
<http://doi.org/10.1109/ICNNSP.2003.1279240> WOS:000189460400042
- C₈₉ R. Andonie, L. Sasu, and V. Beiu: Fuzzy ARTMAP with Relevance Factor
 IEEE International Joint Conference on Neural Networks IJCNN'03
 Portland, OR, USA, July 20-24, 2003 1975–1980
<https://doi.org/10.1109/IJCNN.2003.1223710> WOS:000184903300357
- C₈₈ V. Beiu: A Survey of Perceptron Circuit Complexity Results
 IEEE International Joint Conference on Neural Networks IJCNN'03
 Portland, OR, USA, July 20-24, 2003 989–994
<http://doi.org/10.1109/IJCNN.2003.1223825> WOS:000184903300179
- C₈₇ V. Beiu, J.M. Quintana, M.J. Avedillo, and R. Andonie
 Differential Implementations of Threshold Logic Gates
 IEEE International Symposium on Signal, Circuits and Systems SCS'03
 Iași, Romania, July 10-11, 2003 489–492
<https://doi.org/10.1109/SCS.2003.1227096> WOS:000186628100124
- C₈₅ V. Beiu: Constructive Threshold Logic Addition – A Synopsis of the Last Decade
 International Conference on Artificial Neural Networks ICANN'03
 Istanbul, Turkey, June 26-29, 2003, Springer LNCS 2714 745–752
https://doi.org/10.1007/3-540-44989-2_89 WOS:000185378100089
- C₈₄ V. Beiu, J.M. Quintana, and M.J. Avedillo: Review of Capacitive Threshold Gate Implementations
 International Conference on Artificial Neural Networks ICANN'03
 Istanbul, Turkey, June 26-29, 2003, Springer LNCS 2714 737–744
https://doi.org/10.1007/3-540-44989-2_88 WOS:000185378100088
- C₈₃ S. Tatapudi, and V. Beiu: Split-Precharge Differential Noise-Immune Threshold Logic Gate
 International Work-Conference on Artificial Neural Networks IWANN'03
 Menorca, Spain, June 3-6, 2003, Springer LNCS 2687 49–56

- https://doi.org/10.1007/3-540-44869-1_7 WOS:000185042300007
- C₇₉ V. Beiu: On the Node Complexity of Threshold Gate Circuits with Sub-Linear Fan-Ins
International Conference on Neural Networks and Soft Computing ICNNSC'02
Zakopane, Poland, June 11-15, 2002, Springer, Advances in Soft Computing vol. 19 143–148
https://doi.org/10.1007/978-3-7908-1902-1_18 WOS:000182433900018
- C₇₇ V. Beiu: On Higher Order Noise Immune Perceptrons
IEEE International Joint Conference on Neural Networks IJCNN'01
Washington, DC, USA, July 14-19, 2001, vol. 1 246–251
<https://doi.org/10.1109/IJCNN.2001.939025> WOS:000172784800045
- C₇₅ V. Beiu: High-Speed Noise Robust Threshold Gates
IEEE International Semiconductor Conference CAS'00
Sinaia, Romania, October 10-14, 2000, vol. 1 **Best Paper Award₆** 79–82
<https://doi.org/10.1109/SMICND.2000.890191> WOS:000168560900009
- C₇₄ V. Beiu: Ultra-Fast Noise Immune CMOS Threshold Gates
IEEE Midwest Symposium on Circuits and Systems MWSCAS'00
Lansing, MI, USA, August 8-11, 2000, vol. 3 1310–1313
<https://doi.org/10.1109/MWSCAS.2000.951456> WOS:000172099300305
- C₇₃ V. Beiu: Neural Addition and Fibonacci Numbers
International Work-Conference on Artificial Neural Networks IWANN'99
Alicante, Spain, June 2-4, 1999, Springer LNCS 1607 198–207
<https://doi.org/10.1007/BFb0100486> WOS:000086108300021
- C₇₂ V. Beiu: On Kolmogorov's Superposition and Boolean Functions
IEEE Brazilian Symposium on Neural Networks SBRN'98
Belo Horizonte, Brazil, December 9-11, 1998 55–60
<http://doi.org/10.1109/SBRN.1998.730994> WOS:000077901600010
- C₆₈ V. Beiu, and K.R. Moore: On Analog Implementation of Discrete Neural Networks
International Workshop on Fuzzy Logic and Intelligent Technologies FLINS'98
Antwerp, Belgium, September 14-16, 1998, World Scientific (ISBN: 981-02-3532-1) 258–265
WOS:000078326600029
- C₆₅ V. Beiu, and H.E. Makaruk: Small Fan-In Is Beautiful
IEEE International Joint Conference on Neural Networks IJCNN'98
Anchorage, AK, USA, May 4-9, 1998, vol. 2 1321–1326
<https://doi.org/10.1109/IJCNN.1998.685966> WOS:000074493400242
- C₆₂ V. Beiu, S. Draghici, and H.E. Makaruk: On Limited Fan-in Optimal Neural Networks
IEEE Brazilian Symposium on Neural Networks IV SBRN
Goiania, Brazil, December 3-5, 1997 19–30
<https://doi.org/10.1109/SBRN.1997.645844> WOS:000071092500004
- C₅₆ V. Beiu: Enhanced Lower Entropy Bounds with Application to Constructive Learning
IEEE EuroMicro-Workshop on Computational Intelligence EuroMicro'97
Budapest, Hungary, September 1-4, 1997 541–548
<https://doi.org/10.1109/EURMIC.1997.617371> WOS:A1997BJ48T00068
- C₅₄ V. Beiu, and T. De Pauw: Tight Bounds on the Size of Neural Networks for Classification Problems
International Work-Conference on Artificial Neural Networks IWANN'97
Lanzarote, Canary Islands, Spain, June 4-6, 1997, Springer LNCS 1240 743–752
<https://doi.org/10.1007/BFb0032533> WOS:000073947300076
- C₅₀ V. Beiu: VLSI Complexity of Threshold Gate COMPARISON **Invited₉**
International Symposium on Neuro-Fuzzy Systems AT'96

- Lausanne, Switzerland, August 29-31, 1996, Aati 161–170
<https://doi.org/10.1109/ISNFS.1996.603834> WOS:A1996BH75U00021
- C₄₇ V. Beiu, and J.G. Taylor: Optimal Mapping of Neural Networks onto FPGAs
 International Workshop on Artificial Neural Networks IWANN'95
 Málaga, Spain, June 7-9, 1995, Springer LNCS 930 822–829
https://doi.org/10.1007/3-540-59497-3_256 WOS:A1995BF02K00108
- C₄₅ V. Beiu, and J.G. Taylor: VLSI Optimal Learning Algorithm
 International Conference on Artificial Neural Networks and Genetic
 Algorithms ICANNGA'95, Alès, France, April 19-21, 1995, Springer 61–64
https://doi.org/10.1007/978-3-7091-7535-4_18 WOS:A1995BE73Z00017
- C₄₄ V. Beiu: Optimal VLSI Implementations of Neural Networks, VLSI-Friendly Learning Algorithms *Invited*,
 Applied Decision Technologies Conference ADT'95, London, UK, April 3-5, 1995 193–207
 WOS:A1996BH07W00018
- C₄₂ V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins
 Placing Feedforward Neural Networks Among Several Circuit Complexity Classes
 World Conference on Neural Networks WCNN'94
 San Diego, CA, USA, June 4-9, 1994, Lawrence Erlbaum & INNS (ISBN 0-8058-1745-X) 584–589
 WOS:A1994BB69E00097
- C₂₉ V. Beiu, J.A. Peperstraete, and R. Lauwereins
 Using Threshold Gates to Implement Sigmoid Nonlinearities
 International Conference on Artificial Neural Networks ICANN'92
 Brighton, UK, September 4-7, 1992, Elsevier 1447–1450
<https://doi.org/10.1016/B978-0-444-89488-5.50133-0> WOS:A1992BX31W00307
- C₂₈ V. Beiu, D.C. Ioan, and M.C. Dumbrava
 Continuous Boltzmann Machines: Theoretical Aspects and Applications
 IEEE European Computer Conference CompEuro'92, Hague, Netherlands, May 4-8, 1992 193–198
<https://doi.org/10.1109/CMPEUR.1992.218510> WOS:A1992BW32W00037
- C₂₅ V. Beiu: Neural Network for Digital Image Enhancement
 International Conference on Artificial Neural Networks ICANN'91
 Espoo, Finland, June 24-28, 1991, Elsevier, vol. 2 1071–1074
<https://doi.org/10.1016/B978-0-444-89178-5.50021-X> WOS:A1991BV08V00173
- C₁₉ V. Beiu, and S. Georgescu: Consideration of Vision Based on Associative Neural Networks
 IEEE Annual European Computer Conference CompEuro'89
 Hamburg, Germany, May 8-12, 1989, vol. 2 121–124
<https://doi.org/10.1109/CMPEUR.1989.93388> WOS:A1989BQ37F00064
- C₁₈ V. Beiu: VLSI Arrays Implementing Parallel Line-Drawing Algorithms
 International Workshop on Parallel Processing by Cellular Automata PARCELLA'88
 Berlin, Germany, October 17-21, 1988, Springer LNCS 342 239–247
https://doi.org/10.1007/3-540-50647-0_114 WOS:A1989AB14600015

3. PHD THESIS

- ... V. Beiu: Neural Networks Using Threshold Gates
 A Complexity Analysis of Their Area- and Time-Efficient VLSI Implementations
PhD dissertation (summa cum laude), Katholieke Universiteit Leuven, Leuven, Belgium
 U.D.C. 621.3.04977: 681.3*C13 (x-27-151779-3), May 1994 1–222

4. BOOKS ROMANIAN PUBLISHING HOUSES**5. CHAPTERS ROMANIAN PUBLISHING HOUSES (NUMBERING IS INVERSE CHRONOLOGICAL)**

- Ch₄ V. Beiu: Entropy, Constructive Neural Learning, and VLSI Efficiency *Invited*
In R. Andonie, and D. Grosu (Eds.): Neural Priorities in Data Transmission and EDA
Tempus SJEPE 8180-94, "Transilvania" Univ. of Braşov, Braşov, Romania, 1998 38–74

6. BOOKS FOREIGN PUBLISHING HOUSES (NUMBERING IS INVERSE CHRONOLOGICAL)

- B₂ V. Beiu, and S. Harous (Eds.): Innovations
IEEE Press, November 2014 (ISBN 9781479972128) 1–132
<https://doi.org/10.1109/INNOVATIONS.2014.6985768>
- B₁ A. Schmid, S. Goel, W. Wang, V. Beiu, and S. Carrara (Eds.): Nano-Net
Springer, LNICS, October 2009 (ISBN 9783642024276) 1–286
<https://doi.org/10.1007/978-3-642-04850-0>

7. CHAPTERS FOREIGN PUBLISHING HOUSES (NUMBERING IS INVERSE CHRONOLOGICAL)

- Ch₈ V. Beiu, L. Zhang, A. Beg, W. Ibrahim, and M. Tache: Axon-Inspired Communication Systems *Invited*
Chapter 15 in J.E. Morris and K. Iniewski (Eds.): Nanoelectronic Device Applications
Handbook, CRC/Taylor & Francis (UK/USA), 2013 (ISBN 9781466565234) 193–208
- Ch₇ A. Beg, M.H. Sulieman, V. Beiu, and W. Ibrahim: Low-Power Reliable Nano Adders *Invited*
Chapter 6 in J.E. Morris and K. Iniewski (Eds.): Nanoelectronic Device Applications
Handbook, CRC/Taylor & Francis (UK/USA), 2013 (ISBN 9781466565234) 67–75
- Ch₆ V. Beiu, W. Ibrahim, and S. Lazarova-Molnar
On Device-level Majority von Neumann Multiplexing *Invited*
Chapter 72 in J.R. Rabuñal et al. (Eds.): Encyclopedia of Artificial Intelligence
IGI Global, USA (Hershey, PA) and UK (London), 2009 (ISBN 9781599048499) 471–479
<https://doi.org/10.4018/978-1-59904-849-9.ch072>
- Ch₅ V. Beiu, and W. Ibrahim: On Computing Nano-Architectures Using Unreliable Nano-Devices *Invited*
Chapter 12 in S.E. Lyshevski (Ed.): Nano- and Molecular-Electronics Handbook
Taylor & Francis (UK/USA), May 2007 (ISBN 9780849385285) 1–49
- Ch₃ V. Beiu: Constant Fan-in Discrete Neural Networks Are VLSI-Optimal
Chapter 12 in S.W. Ellacott, J.C. Mason, and I.J. Anderson (Eds.)
Mathematics of Neural Networks Models, Algorithms and Applications
Kluwer Academic, Boston, MA, USA, 1997 (ISBN 9781461377948) 89–94
https://doi.org/10.1007/978-1-4615-6099-9_12
- Ch₂ V. Beiu: Digital Integrated Circuit Implementations (of Neural Networks) *Invited*
Chapter E1.4 in E. Fiesler, and R. Beale (Eds.): Handbook of Neural Computations
Institute of Physics, New York, NY, USA, 1996 (ISBN 9780750303125) E1.4.1–34
- Ch₁ V. Beiu: Optimal VLSI Implementations of Neural Networks *Invited*
Chapter 18 in J.G. Taylor (Ed.): Neural Networks and Their Applications
John Wiley & Sons, Chichester, UK, 1996 (ISBN 9780471962823) 255–276

8. BDI ARTICLES (NUMBERING IS INVERSE CHRONOLOGICAL)

- J₃₇ M. Tache, M. Balas, and V. Beiu
When Non-Gaussian Distributions Have to Be Considered
Theory and Applications of Mathematics & Computer Science *Accepted*
- J₃₆ V. Dragoi, S.R. Cowell, M. Nagy, and V. Beiu
A Preliminary Investigation of Matchstick Minimal Networks
Theory and Applications of Mathematics & Computer Science *Accepted*
- J₃₂ S.R. Cowell, M. Nagy, and V. Beiu
A Proof of a Generic Fibonacci Identity from Wolfram's MathWorld
Theory and Applications of Mathematics & Computer Science, vol. 8, no. 1, Apr. 2018 60–63
<http://www.uav.ro/applications/se/journal/index.php/TAMCS/article/view/175>
- J₂₉ V. Beiu, and M. Tache
On Threshold Voltage Variation-Tolerant Designs
Theory and Applications of Mathematics & Computer Science, vol. 7, no. 1, Apr. 2017 47–58
http://www.uav.ro/stiinte_exacte/journal/index.php/TAMCS/article/view/159
- J₂₀ V. Beiu, B.A.M. Madappuram, P.M. Kelly, and L.J. McDaid
On Two-layer Brain-inspired Hierarchical Topologies — A Rent's Rule Approach
Transactions on High-Performance Embedded Architecture and Compilers (HiPEAC) IV
P. Stenström (Ed.), Springer LNCS 6769, Jan. 2011 311–333
https://doi.org/10.1007/978-3-642-24568-8_16
- J₁₃ V. Beiu: On VLSI-Optimal Neural Computations
Journal of Control Engineering & Applied Informatics, vol. 4, no. 2, Feb. 2002 (IF later) 5–20
<http://www.ceai.srait.ro/index.php?journal=ceai&page=article&op=view&path%5B%5D=89>
- J₁₂ V. Beiu: On Optimal Computations Using Perceptrons
Journal of Control Engineering & Applied Informatics, vol. 4, no. 1, Jan. 2002 (IF later) 33–43
<http://www.ceai.srait.ro/index.php?journal=ceai&page=article&op=view&path%5B%5D=84>
- J₈ V. Beiu: Reduced Complexity Constructive Learning Algorithm
Neural Network World, vol. 8, no. 1-3, Jan. 1998 (IF later, SJR later) 1–38
- J₆ V. Beiu: Entropy Bounds for Classification Algorithms
Neural Network World, vol. 6, no. 4, Jul. 1996 (IF later, SJR later) 497–505
- J₅ V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins: Close Approximations of Sigmoid
Functions by Sum of Steps for VLSI Implementation of Neural Networks
Scientific Annals of "Al. I. Cuza" University of Iași, vol. 40, no. 3, 1994 (IF later) 5–34
- J₄ V. Beiu, D.C. Ioan, and M.C. Dumbrava
Continuous Boltzmann Machines: Theoretical Aspects and Applications
Neural Network World, vol. 2, no. 2, Mar. 1992 (IF later, SJR later) 201–226
- J₃ V. Beiu: From Systolic Arrays to Neural Networks
Scientific Annals of "Al. I. Cuza" University of Iași, vol. 35, no. 4, 1989 (IF later) 375–385
- J₂ V. Ivanov, and V. Beiu: Search Algorithm for an Inference Machine: Software and Hardware
UPB Scientific Bulletin, Control & Computers, vol. AC-50, 1988 (SJR later) 83–96
- J₁ E. Oltean, and V. Beiu: Numerical Aspects in the Implementation of Self-Tuning Algorithms
UPB Scientific Bulletin, Control & Computers, vol. AC-48, 1986 (SJR later) 79–92

Remark: The following 4 reports are available on arXiv

- R₄ V. Dragoi, S.R. Cowell, and V. Beiu
Tight Bounds on the Coefficients of Consecutive k -out-of- n :F Systems

- Tech. Rep. arXiv, Discrete Mathematics (cs.DM), 27 Mar. 2020 1–10
<https://arxiv.org/abs/2003.12419>
- R₃ V. Dragoi, and V. Beiu
 Fast Reliability Ranking of Matchstick Minimal Networks
 Tech. Rep. arXiv, Discrete Mathematics (cs.DM), 4 Nov. 2019 1–16
<https://arxiv.org/abs/1911.01153>
- R₂ M. Nagy, S.R. Cowell, and V. Beiu
 Survey of Cubic Fibonacci Identities – When Cuboids Carry Weights
 Tech. Rep. arXiv, History and Overview (math.CO), 15 Feb. 2019 1–14
<https://arxiv.org/abs/1902.05944>
- R₁ L. Dauş, V. Beiu, S.R. Cowell, and P. Poulin
 Brick-Wall Lattice Paths and Applications
 Tech. Rep. arXiv, Combinatorics (math.CO), 14 Apr. 2018 1–16
<https://arxiv.org/abs/1804.05277>

9. BDI CONFERENCE ARTICLES (NUMBERING IS INVERSE CHRONOLOGICAL)

- C₂₀₇ V. Dragoi, V. Beiu, and D. Bucerzan
 Vulnerabilities of the McEliece Variants Based on Polar Codes
 International Conference on Security for Information Technology & Communications SecICT'18
 Bucharest, Romania, November 08-09, 2018
 In J.-L. Lanet and C. Toma (Eds.): SecITC 2018, Springer, LNCS 11359, 2019 376–390
https://doi.org/10.1007/978-3-030-12942-2_29
- C₂₀₃ V. Dragoi, S.R. Cowell, M. Nagy, and V. Beiu
 Matchstick Minimal Circuits
 International Symposium Research and Education in an Innovation Era ISREIE'18
 Section Mathematics & Computer Science (ISSN 2065-2569)
 Arad, Romania, May 17-20, 2018 112–121
<https://uav.ro/en/conferences/isreie-2018>
- C₁₈₂ V. Beiu, and L. Dauş
 Deciphering the Reliability Scheme of the Neurons – One Ion Channel at a Time *Invited*₂₆
 International Conference on Bio-inspired Info & Communication Technology BICT'14
 Boston, MA, USA, December 1-3, 2014 182–187
<https://doi.org/10.4108/icst.bict.2014.257905>
- C₁₆₇ P. Santagati, and V. Beiu: A Mathematical Model for the Analysis of the Johnson-Nyquist
 Noise on the Reliability of Nano-Communications
 International Conference on Bio-Inspired Models of Network, Information,
 and Computing Systems BIONETICS'12, Lugano, Switzerland, December 10-12, 2012
 In G.A. Di Caro, and G. Theraulaz (eds.), Springer, LNICST vol. 134, July 2014 49–62
https://doi.org/10.1007/978-3-319-06944-9_4
- C₁₅₁ L. Zhang, H. Elsayed, and V. Beiu
 A Position-Based Broadcast Relay Approach in Mobile Vehicle-to-Vehicle Network
 International Conference on Wireless Networks ICWN'10 (part of WorldComp'10)
 Las Vegas, NV, USA, July 12-15, 2010 611–616
- C₁₄₂ V. Beiu, and W. Ibrahim: On CMOS Circuit Reliability from the MOSFETs and the Input Vectors
 IEEE/IFIP International Conference on Dependable Systems and Networks DSN'09
 Estoril, Lisbon, Portugal, June 29 - July 2, 2009
http://www.laas.fr/WDSN09/WDSN09_files/Texts/WDSN09-2-2-Beiu.pdf

- C₁₃₆ V. Beiu: Electrons Behaving Badly — Quo Vadis Nano-architecture? *Invited*₂₀
 International Symposium on Information Electronics Systems IES'08
 Sendai, Japan, July 14-15, 2008 24–27
http://www.ecei.tohoku.ac.jp/gcoe/en/sympo/sympo_2nd/invited.html
- C₁₃₅ S. Lazarova-Molnar, and V. Beiu: Reliability Modeling of Circuits with Multi-State Aging Gates
 Modeling & Simulation – Methodology, Tools, Software Applications M&S–MTSA'08
 Edinburgh, UK, June 16-19, 2008 43–47
- C₁₂₈ V. Beiu, H. Amer, and M. McGinnity *Invited*₁₉
 On Global Communications for Nano-Architectures – Brain versus Rent's Rule
 International Conference on Design of Circuits and Integrated Systems DCIS'07
 Seville, Spain, November 21-23, 2007 305–310
<http://www2.imse-cnm.csic.es/dcis07/>
- C₁₁₉ V. Beiu: Grand Challenges of Nanoelectronics and Possible Architectural Solutions *Invited*₁₈
 IEEE International Symposium on Multiple Valued Logic ISMVL'07
 Oslo, Norway, May 14-16, 2007 a(1–7)
<https://doi.org/10.1109/ISMVL.2007.27>
- C₁₁₈ V. Beiu, and W. Ibrahim: Why Inverters and Small Fan-in Voters Are the Most Promising Gates
 IEEE International Workshop on Post-Binary ULSI Systems ULSIWS'07
 Oslo, Norway, May 13, 2007 3–10
http://ismvl07.ifi.uio.no/docs/Program_ULSIWS07.pdf
- C₁₁₃ V. Beiu: The Quest for Practical Redundant Computations *Invited*₁₇
 IEEE International Conference on Microelectronics ICM'05
 Islamabad, Pakistan, December 13-15, 2005 xix
<https://doi.org/10.1109/ICM.2005.1590021>
- C₁₁₂ S. Aunet, Y. Berg, and V. Beiu: Ultra Low-Power Redundant Logic Based on Majority-3 Gates
 IFIP International Conference on VLSI System-on-Chip VLSI-SoC'05
 Perth, Australia, October 17-19, 2005 553–558
 Springer, IFIP 240, ISBN: 978-0-387-73660-0
- C₈₆ Z. Zhou, D.J. Betwoski, X. Li, G. La Rue, and V. Beiu
 High Performance Direct Digital Frequency Synthesizers
 Biennial University/Government/Industry Microelectronics Symposium UGIM'03
 Boise, ID, USA, June 30 - July 2, 2003 368–369
<https://doi.org/10.1109/UGIM.2003.1225770>
- C₈₂ R. Andonie, L.M. Sasu, and V. Beiu
 A Modified Fuzzy ARTMAP Architecture for Incremental Learning Function Approximation
 International Conference on Neural Networks and Computational Intelligence NCI'03
 Cancun, Mexico, May 19-21, 2003, ACTA Press 124–129
<http://www.actapress.com/Abstract.aspx?paperId=13609>
- C₈₁ V. Beiu: On Existential and Constructive Neural Complexity Results
 International Conference on Neural Networks and Computational Intelligence NCI'03
 Cancun, Mexico, May 19-21, 2003, ACTA Press 63–72
<http://www.actapress.com/Abstract.aspx?paperId=13599>
- C₈₀ V. Beiu, J.M. Quintana, and M.J. Avedillo: Review of Differential Threshold Gate Implementations
 International Conference on Neural Networks and Computational Intelligence NCI'03
 Cancun, Mexico, May 19-21, 2003, ACTA Press 44–49
<http://www.actapress.com/Abstract.aspx?paperId=13596>
- C₇₈ V. Beiu: Depth-Size Tradeoffs for Threshold Gate Circuits

	Italian Workshop on Neural Networks WIRN-Vietri'02 Vietri sul Mare, Italy, May 31 - June 1, 2002	88–91
C ₇₆	V. Beiu: On VLSI-Optimal Neural Computations International Conference on Control Systems and Computer Science CSCS-13 Bucharest, Romania, May 31 - June 3, 2001	450–455
C ₇₁	V. Beiu: Larger Bases and Mixed Analog/Digital Neural Networks International Conference on Artificial Neural Networks in Engineering ANNIE'98 St. Louis, MI, USA, November 1-4, 1998. In C.H. Dagli et al. (Eds.), ASME Press	63–70
C ₇₀	V. Beiu: 2D Neural Hardware vs 3D Biological Ones ICSC/IFAC International Symposium on Neural Computations NC'98 Vienna, Austria, September 23-25, 1998, ICSC Academic Press http://www.icsc.ab.ca/publications/list_nc98.html	<i>Invited</i> ₁₃ 37–45
C ₆₉	V. Beiu: On Automatic Synthesis of Analog/Digital Circuits International Symposium on Nonlinear Theory and Its Applications NOLTA'98 Crans-Montana, Switzerland, September 14-17, 1998, vol. 2	799–802
C ₆₇	V. Beiu: Implementing Size-Optimal Discrete Neural Networks Requires Analog Circuitry European Signal Processing Conference EuSiPCo'98 Rhodes, Greece, September 8-11, vol. 3, Typorama (ISBN: 978-960-7620-06-4)	1325–1328
C ₆₆	V. Beiu: Neural Inspired Parallel Computations Require Analog Processors International Conference on Parallel Computing and Electrical Engineering PARELEC'98 Bialystok, Poland, September 2-5, 1998	<i>Invited</i> ₁₂ 39–53
C ₆₄	V. Beiu: How to Build VLSI-Efficient Neural Chips ICSC International Symposium on Engineering of Intelligent Systems EIS'98 Tenerife, Canary Islands, Spain, February 9-13, 1998, ICSC Academic Press, vol. 2 http://www.icsc.ab.ca/publications/list_eis98.html	<i>Invited</i> ₁₁ 66–75
C ₆₃	V. Beiu, and H.E. Makaruk: Deeper and Sparser Nets Are Optimal ICSC International Symposium on Engineering of Intelligent Systems EIS'98 Tenerife, Canary Islands, Spain, February 9-13, 1998, ICSC Academic Press, vol. 2 http://www.icsc.ab.ca/publications/list_eis98.html	<i>Invited</i> ₁₀ 59–65
C ₆₁	V. Beiu, and H.E. Makaruk: Computing Volumes of n -Dimensional Complexes International Symposium on Nonlinear Theory and Its Applications NOLTA'97 Honolulu, HI, USA, November 29 - December 3, 1997, IEICE Press, vol. 1	417–420
C ₆₀	S. Draghici, V. Beiu, and I.K. Sethi: A VLSI Optimal Constructive Algorithm International Conference on Artificial Neural Networks in Engineering ANNIE'97 St. Louis, MI, USA, November 9-12, 1997, ASME Press	145–151
C ₅₉	V. Beiu: When Reduced Connectivity Neural Networks Are Complexity Optimal? International Workshop on Neural Networks HELNET'97 Montreux, Switzerland, October 4-6, 1997, VU University Press	109–116
C ₅₈	V. Beiu, and S. Draghici: On Sparsely Connected Optimal Neural Networks International Conference on Microelectronics for Neural Networks MicroNeuro'97 Dresden, Germany, September 24-26, 1997, Sächsisches Druck- und Verlagshaus	56–63
C ₅₇	V. Beiu, and S. Draghici: Limited Weights Neural Networks – Very Tight Entropy Based Bounds ICSC International Symposium on Soft Computing SOCO'97 Nîmes, France, September 17-19, 1997, ICSC Academic Press http://www.icsc.ab.ca/publications/list_soco97.html	111–118
C ₅₅	V. Beiu: Optimization of Circuits Using a Constructive Neural Network Learning Algorithm	

	International Conference on Engineering Applications of Neural Networks EANN'97 Stockholm, Sweden, June 16-18, 1997, Åbo Akademis	291–194
C ₅₃	V. Beiu: When Constants Are Important International Conference on Control System and Computer Science CSCS-11 Bucharest, Romania, May 28-31, 1997, vol. 2	106–111
C ₅₂	S. Draghici, and V. Beiu: Entropy Based Comparison of Neural Networks for Classification Italian Workshop on Neural Nets WIRN-Vietri'97 Vietri sul Mare, Salerno, Italy, May 22-24, 1997, Springer https://doi.org/10.1007/978-1-4471-1520-5_6	124–132
C ₅₁	V. Beiu: New VLSI Complexity Results for Threshold Gate COMPARISON Brazilian Symposium on Neural Networks III SBRN Recife, Brazil, November 12-14, 1996, UFPE-DI	251–258
C ₄₉	V. Beiu, and J.G. Taylor: Direct Synthesis of Neural Networks International Conference on Microelectronics for Neural Networks MicroNeuro'96 Lausanne, Switzerland, February 12-14, 1996 https://doi.org/10.1109/MNNFS.1996.493800	257–264
C ₄₈	J.C. Lemm, V. Beiu, and J.G. Taylor Density Estimation as a Preprocessing Step for Constructive Algorithms Annual Symposium on Neural Network SNN'95 Nijmegen, The Netherlands, September 14-15, 1995, Springer https://doi.org/10.1007/978-1-4471-3087-1_41	213–216
C ₄₆	V. Beiu, and J.G. Taylor: Area-Efficient Constructive Learning Algorithm International Conference on Control System and Computer Science CSCS-10 Bucharest, Romania, May 24-26, 1995, vol. 3	<i>Invited</i> ₈ 293–310
C ₄₃	V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins Addition Using Constrained Threshold Gates International Conference on Technical Informatics ConTI'94 Timișoara, Romania, November 16-19, 1994	<i>Invited</i> ₆ 166–177
C ₄₁	V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins On the Circuit Complexity of Feedforward Neural Networks International Conference on Artificial Neural Networks ICANN'94 Sorrento, Italy, May 26-29, 1994, Springer https://doi.org/10.1007/978-1-4471-2097-1_121	521–524
C ₄₀	V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins Area-Time Performances of Some Neural Computations International Symposium on Signal Processing, Robotics, & Artificial Neural Networks SPRANN'94, Lille, France, April 25-27, 1994, GERF EC (ISBN: 2950290833)	664–668
C ₃₉	V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins VLSI Complexity Reduction by Piece-Wise Approximation of the Sigmoid Function European Symposium on Artificial Neural Networks ESANN'94 Brussels, Belgium, April 20-22, 1994, D factio https://www.elen.ucl.ac.be/esann/proceedings/papers.php?ann=1994#ES1994-529	<i>Invited</i> ₅ 181–186
C ₃₈	V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins Learning from Examples and VLSI Implementation of Neural Networks European Meeting on Cybernetics and System Research EMCSR'94 Vienna, Austria, April 5-8, 1994, World Scientific (ISBN: 9789814534376)	<i>Invited</i> ₄ 1767–1774
C ₃₇	V. Beiu, J.A. Peperstraete, and R. Lauwereins	

- Enhanced Threshold Gate Fan-In Reduction Algorithms
International Conference for Young Computer Scientists ICYCS'93
Beijing, China, July 15-17, 1993, Tsinghua Press (ISBN: 7-302-00888) 3.39–3.42
- C₃₆ V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins
Overview of Some Efficient Threshold Gate Decomposition Algorithms *Invited₃*
International Conference on Control System and Computer Science CSCS-9
Bucharest, Romania, May 25-28, 1993, Joint Printing House, vol. 1 458–469
- C₃₅ D.O. Creteanu, V. Beiu, J.A. Peperstraete, and R. Lauwereins
Systolic Pattern Recognition Based on a Neural Network Algorithm
International Conference on Artificial Neural Networks and Genetic
Algorithms ICANNGA'93, Innsbruck, Austria, April 13-16, 1993, Springer 137–144
https://doi.org/10.1007/978-3-7091-7533-0_22
- C₃₄ V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins
Efficient Decomposition of Comparison and Its Applications
European Symposium on Artificial Neural Networks ESANN'93
Brussels, Belgium, April 7-9, 1993, D factio 45–50
<https://www.elen.ucl.ac.be/esann/proceedings/papers.php?ann=1993#ES1993-507>
- C₃₃ V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins
COMPARISON and Threshold Gate Decomposition
International Conference on Microelectronics for Neural Networks MicroNeuro'93
Edinburgh, UK, April 6-8, 1993, Pub. UnivEd 83–90
- C₃₂ V. Beiu, J.A. Peperstraete, and R. Lauwereins
Enhanced Threshold Gate Fan-in Reduction Algorithm *Invited₂*
Interdisciplinary Centrum for Neural Networks ICNN'92
Leuven, Belgium, November 19, 1992, KUL Press 65–70
- C₃₁ V. Beiu, J.A. Peperstraete, and R. Lauwereins: Simpler Neural Networks by Fan-in Reduction
IEEE International Joint Conference on Neural Networks IJCNN'92
Beijing, China, November 3-6, 1992, vol. 3 204–209
- C₃₀ V. Beiu, J.A. Peperstraete, and R. Lauwereins: Algorithms for Fan-in Reduction
International Conference on Neural Networks and Their Applications NeuroNimes'92
Nîmes, France, November 2-6, 1992, EC2 589–600
- C₂₇ V. Beiu, D.C. Ioan, M.C. Dumbrava, and O. Robciuc
Physical Fields Determination Using Continuous Boltzmann Machines
IASTED International Symposium APPLIED INFORMATICS'92
Innsbruck, Austria, February 10-12, 1992, Acta Press 284–287
- C₂₆ S. Georgescu, and V. Beiu: Optimal Reconstruction from Sampled Data with Parallel Structures
ISMM International Workshop on Parallel Computing ParComp'91
Trani, Italy, September 10-13, 1991, Anaheim: Acta Press (ISBN: 0889861471) 260–263
- C₂₄ V. Beiu: NeuroSim – A Neural Network Simulator
International Conference on Control System and Computer Science CSCS-8
Bucharest, Romania, May 22-25, 1991 28–36
- C₂₃ V. Beiu: Neural Network Priority Queue *Invited₁*
International Workshop on Parallel Processing by Cellular Automata PARCELLA'90
Berlin, Germany, September 19-21, 1990, Akademie Verlag 130–136
- C₂₂ V. Beiu, A. Florea, and S. Georgescu: The Facilities of the NeuroSim Environment
International Symposium on Informatics INFO-IASI'89, Iași, Romania, October 19-21, 1989 196–202

C ₂₁	V. Beiu, and S. Georgescu: Recognition of Moving Objects Using NeuroSim International Symposium on Informatics INFO-IASI'89, Iași, Romania, October 19-21, 1989	186–195
C ₂₀	A. Petrescu, and V. Beiu: The "Hello VLSI" CAD Environment IEEE Annual Conference on Semiconductors CAS'89, Sinaia, Romania, October 11-14, 1989	78–82
C ₁₇	V. Beiu: A Smart-Memory for Set-Structure Processing International Symposium on Informatics INFO-IASI'87 Iași, Romania, October 8-10, 1987, vol. 1	404–413
C ₁₆	V. Beiu: VLSI Arrays Implementing Parallel Line-Drawing Algorithms International Symposium on Informatics INFO-IASI'87 Iași, Romania, October 8-10, 1987, vol. 1	395–403
C ₁₅	V. Beiu: Smart VLSI Memory Chips Implementing Elementary Operations on Lists International Conference on Control System and Computer Science CSCS-7 Bucharest, Romania, May 27-30, 1987, vol. 3	16–22
C ₁₄	E. Oltean, and V. Beiu: Adaptive Kalman Filtering – Implementation of a Dedicated Structure International Conference on Control System and Computer Science CSCS-7 Bucharest, Romania, May 27-30, 1987, vol. 2	21–26
C ₁₃	V. Beiu, and C. Constantinescu: Fault-Tolerant Systolic Arrays for Antialiasing IEEE Annual European Computer Conference CompEuro'87 Hamburg, Germany, May 11-15, 1987	720–723
C ₁₂	V. Beiu: Self-Testable and Self-Repairable Antialiasing Unit International MICROELECTRONICS'86 Conference Plovdiv, Bulgaria, October 23–25, 1986, vol. 2	183–195
C ₁₁	V. Beiu, and A. Neagu: Algorithm for Adding Universal Represented Real (URR) Numbers International Symposium on Informatics INFO-IASI'85 Iași, Romania, October 18-19, 1985, vol. 2	760–768
C ₁₀	V. Beiu: Dedicated Computing Unit for Antialiasing International Symposium on Informatics INFO-IASI'85 Iași, Romania, October 18-19, 1985, vol. 2	590–599
C ₉	V. Beiu, and I. Roșu: VLSI Implementation of a Self-Testable Real Content Addressable Memory International Conference on Control System and Computer Science CSCS-6 Bucharest, Romania, May 22-25, 1985, vol. 2	400–405
C ₈	V. Beiu, A. Petrescu, and I. Roșu Design of Hierarchically Organized Memories for VLSI Implementation International Conference on Control System and Computer Science CSCS-6 Bucharest, Romania, May 22-25, 1985, vol. 2	69–75
C ₇	I. Roșu, V. Beiu, and T. Kappel: An Algorithm for Priorities Evaluation in a Statistical Multiplexer International Conference on Control System and Computer Science CSCS-5 Bucharest, Romania, June 8-11, 1983, vol. 2	368–372
C ₆	V. Beiu: High Speed Algorithm for Executing the MOD Instruction National Conference on Electronics, Telecommunication, Control and Computers CNETAC'82 Bucharest, Romania, November 17-19, 1982	175–179
C ₅	A. Aurelian, V. Beiu, and R. Muntean: Programmable Binary Multipliers in the Range $2^2 : 2^{10}$ Students Scientific Research Conference Bucharest, Romania, May 17-18, 1980	Best Paper Award ₅ 721–725
C ₄	V. Beiu, R. Muntean, and A. Aurelian: Graphic Workstation – RAM/ROM Character Generator Students' Scientific Research Conference	Best Paper

- Bucharest, Romania, May 17-18, 1980 *Award₄* 726–730
- C₃ R. Munteanu, A. Aurelian, and V. Beiu: Ultra High Speed TTL Unit for a Graphic Workstation *Best Paper*
 Students Scientific Research Conference
 Bucharest, Romania, May 17-18, 1980 *Award₃* 731–735
- C₂ V. Beiu: Field Effect Optoelectronic Equipments *Best Paper*
 Students' Scientific Research Conference
 Bucharest, Romania, May 13-14, 1977 *Award₂* 476–480
- C₁ V. Beiu: Bistable Cholesteric Mixtures with Positive Dielectric Anisotropy *Best Paper*
 Students Scientific Research Conference
 Bucharest, Romania, May 13-14, 1977 *Award₁* 471–475

Remark: The following "other conferences" have presented

- O₅₁ R.-M. Beiu, M. M. Balas, V. E. Balas, and V. Beiu
 Seeing is Believing
 International Summit on Optics, Photonics and Laser Technologies OPTICS&LASERS'19
 San Francisco, CA, USA, June 03-05, 2019
- O₅₀ M. Nagy, S. R. Cowell, and V. Beiu
 Optimal Cubic Fibonacci Identities for 3D Packing
 International Symposium Research and Education in Innovation Era ISREIE'19
 Arad, Romania, May 23-25, 2019
- O₄₉ M. Tache, S. R. Cowell, and V. Beiu
 Turning Sizing on Its Head and More
 International Symposium Research and Education in Innovation Era ISREIE'19
 Arad, Romania, May 23-25, 2019
- O₄₈ R.-M. Beiu, and V. Beiu
 Sidestepping the Bounds of Diffraction
 International Symposium Research and Education in Innovation Era ISREIE'19
 Arad, Romania, May 23-25, 2019
- O₄₇ G. Cristescu, V. Dragoi, and V. Beiu
 Cubic Spline Approximation of the Reliability Polynomials of Two Dual Hammock Networks
 International Symposium Research and Education in Innovation Era ISREIE'19
 Arad, Romania, May 23-25, 2019
- O₄₆ L. Hamad, A. Fahad, A. Saeed, F. Kharbash, and V. Beiu
 On Reliability-Enhanced Quantum Cellular Automata (QCA) Designs
 UAEU Annual Research & Innovation Conference ARIC'15
 Al Ain, UAE, November 24-25, 2015
- O₄₅ L. Daus, and V. Beiu: A Survey of Consecutive- k -out-of- n Systems Bounds
 IEEE International Symposium on Multiple-Valued Logic ISMVL'14
 International Workshop on Post-Binary ULSI Systems ULSIWS'14
 Bremen, Germany, May 18-21, 2014
- O₄₄ M. Tache, V. Beiu, W. Ibrahim, F. Kharbash, and M. Alioto: Sizing for Static Noise Margins Revisited
 European Workshop on CMOS Variability VARI'13/PATMOS'13
 Karlsruhe, Germany, September 9-11, 2013
- O₄₃ V. Beiu, W. Ibrahim, A. Beg, and M. Tache: On Sizing Transistors for Threshold Voltage Variations
 International Workshop on Design for Reliability DFR'12 (in conjunction with HiPEAC'12)
 Paris, France, January 23-25, 2012
http://www.cs.ucy.ac.cy/carch/DFR2012/presentations/S2_3.pdf

- O₄₂ V. Beiu, and W. Ibrahim: NAND Multiplexing Down to Nuts and Bolts
International Conference on Ultimate Integration on Silicon ULIS'10
Glasgow, UK, March 17-19, 2010
- O₄₁ B.A.M. Madappuram, V. Beiu, and T.M. McGinnity
On Brain-inspired Hybrid Network Topologies for Future Nano-architectures
UAEU Annual Research Conference ARC-9, Al Ain, UAE, April 21-23, 2008 **Best Paper Award**
- O₄₀ S. Lazarova-Molnar, and V. Beiu
Mapping the Proxel-Based Method to Reliability Analysis of Nano-architectures
UAEU Annual Research Conference ARC-9, Al Ain, UAE, April 21-23, 2008
- O₃₉ R.M. Beiu, C.D. Stanescu, and V. Beiu
Nanostructured Fiber Optics as Highly Sensitive Mechanical Sensors
International Trends in NanoTechnology Conference TNT'07
San Sebastian, Spain, September 3-7, 2007 **Invited**
- O₃₈ W. Ibrahim, and V. Beiu
A Hybrid Monte-Carlo and Numerical Simulations Approach for Future Nano-circuits Reliability Calculation
International Trends in NanoTechnology Conference TNT'07
San Sebastian, Spain, September 3-7, 2007
- O₃₇ S. Lazarova-Molnar, V. Beiu, and W. Ibrahim: Proxels for Reliability Assessment of Future Nano-Circuits
International Trends in NanoTechnology Conference TNT'07
San Sebastian, Spain, September 3-7, 2007
- O₃₆ H. Amer, and V. Beiu: On Global Communications for Nano-Architectures – Brain versus Rent's Rule
International Trends in NanoTechnology Conference TNT'07
San Sebastian, Spain, September 3-7, 2007
- O₃₅ B.A.M. Madappuram, and V. Beiu
Using Standing Waves for Communications Might Work for Crossbar Architectures
International Trends in NanoTechnology Conference TNT'07
San Sebastian, Spain, September 3-7, 2007
- O₃₄ M.H. Sulieman, and V. Beiu: Investigating the Reliability of Single-Electron-Technology Gates and Circuits
UAEU Annual Research Conference ARC-8, Al Ain, UAE, April 23-25, 2007
- O₃₃ V. Beiu, J. Nyathi, and S. Aunet
Sub-Pico (Femto) Joule Switching: High-Speed Reliable CMOS Circuits Are Feasible
International Conference on Innovations in Information Technology IIT'05
Dubai, UAE, September 26-28, 2005
http://www.it-innovations.ae/iit005/proceedings/articles/E_5_IIT05_Beiu.pdf
- O₃₂ V. Beiu, S. Aunet, R. Rydberg III, A. Djupdal, and J. Nyathi
The Vanishing Majority Gate – Trading Power and Speed for Reliability
IEEE International Workshop on Design and Test of Defect-Tolerant
Nanoscale Architectures NanoArch'05, Palm Springs, CA, USA, May 1, 2005
- O₃₁ J. Nyathi, V. Beiu, and S. Aunet: Sub Femto Joule Switching – High Speed Reliable CMOS Circuits Are Feasible
ASILOMAR Conference on Signal, Systems and Computers
Pacific Groove, CA, USA, November 7-10, 2004
- O₃₀ J. Nyathi, V. Beiu, and S. Aunet
Femto Joule Switching – Review of Low Energy Design Styles for the Nano Era
International Symposium on Nano and Giga Challenges in Nanoelectronics NGCM'04
Krakow, Poland, September 13-17, 2004 **Invited**
- O₂₉ V. Beiu, U. Rückert, S. Roy, and J. Nyathi: On Nanoelectronic Architectural Challenges and Plausible Solutions

- International Symposium on Nano and Giga Challenges in Nanoelectronics NGCM'04
Krakow, Poland, September 13-17, 2004
- O₂₈ V. Beiu, and A. Zawadzki: Why VLSI/Nano Library Design Should Use Kolmogorov's Superpositions
International Symposium on Nano and Giga Challenges in Nanoelectronics NGCM'04
Krakow, Poland, September 13-17, 2004
- O₂₇ V. Beiu: On Biological and Hardware Neural Networks *Invited*
International Joint Meeting AMS-SMM, Denton, TX, USA, May 19-22, 1999
- O₂₆ V. Beiu, J. Frigo, and K.R. Moore: Why the Nervous Networks Are Reliable
International Symposium on Artificial Intelligence and Adaptive Systems CIMAFA'99
Havana, Cuba, March 24-28, 1999
- O₂₅ V. Beiu, J. Frigo, and K.R. Moore: On the Reliability of Nervous Nets
International Conference on Computational Intelligence for Modeling
Control and Automation CIMCA'99, Vienna, Austria, February 17-19, 1999
- O₂₄ S. Draghici, and V. Beiu: On Issues Related to VLSI Implementations of Neural Networks
International Conference on Cognitive and Neural Systems CNS'98
Boston, MA, USA, May 27-30, 1998
- O₂₃ V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins
Digital Implementation of Neural Networks Using Threshold Gates
International Conference Romania and Romanians in Contemporary Science ICRRCS'94
Sinaia, Romania, May 24-27, 1994
<http://citeseerx.ist.psu.edu/viewdoc/citations;jsessionid=E6CF9AE07D31AEDC41844D7E839B9EAB?doi=10.1.1.30.8504>
- O₂₂ D.O. Creteanu, and V. Beiu: Systolic Pattern Recognition System
International Conference on Fuzzy Systems and Artificial Intelligence IFSAI'92
Iasi, Romania, October 28-31, 1992
- O₂₁ V. Beiu, D.C. Ioan, M. Dumbrava, and O. Robciuc *Invited*
Physical Fields Determination Using Continuous Boltzmann Machines
Symposium on Parallel Computing, Bucharest, Romania, December 10-11, 1991
- O₂₀ V. Beiu: Motion Detection with Neural Networks
International Conference on Industrial and Applied Mathematics ICIAM'91
Washington DC, USA, July 8-12, 1991
- O₁₉ V. Beiu: Neural Network Solutions for Motion Detection
International Symposium on Applied Informatics, Innsbruck, Austria, February 18-21, 1991
- O₁₈ A. Florea, V. Beiu, and S. Georgescu: Expert System Development with a Neural Network Simulator
International Conference on AI and Control Systems for Robots AICSR'89
Strbskoe Pleso, Czechoslovakia, November 6-10, 1989
- O₁₇ V. Beiu: From Systolic Arrays to Neural Networks *Invited*
International Symposium on Informatics INFO-IASI'89
Iasi, Romania, October 19-21, 1989
- O₁₆ M. Constantinescu, and V. Beiu: Theoretical Aspects of Parallel Algorithms for Histogram Modification
International Conference on Computer Systems MICROSYSTEM'89
Carlsbad (Karlovy Vary), Czechoslovakia, September 18-21, 1989
- O₁₅ V. Beiu, and S. Georgescu: Neural Network Models of Vision
IAPR Workshop on Computer Vision, Tokyo, Japan, October 12-14, 1988
- O₁₄ A. Florea, and V. Beiu: Expert Decisions Using Neural Models
Conference on Electronics, Telecommunication, Control and Computers CNETAC'88

Bucharest, Romania, December 7-9, 1988

- O₁₃ V. Beiu: Hierarchical Memory Enhanced with List Processing Facilities
International Conference on Computer Systems MICROSYSTEM'88
Bratislava, Czechoslovakia, August 30 - September 1, 1988
- O₁₂ V. Beiu: Parallel Line-Drawing Algorithms
International Conference on Computer Systems MICROSYSTEM'88
Bratislava, Czechoslovakia, August 30 - September 1, 1988
- O₁₁ V. Beiu, M. Ionescu, E. Paşol, and L. Zuzu: VLSI Implementation of a Statistical Multiplexer
International Symposium Mini and Microcomputers ISMM-MIMI'87
Lugano, Switzerland, June 29 - July 2, 1987
- O₁₀ V. Beiu, M. Ionescu, E. Paşol, and L. Zuzu: Adaptive Multiplexing Algorithm and Its Possible VLSI Implementation
Mediterranean Electrotechnical Conference MELECON'87, Rome, Italy, March 24-26, 1987
- O₉ V. Beiu: Smart Image Memory for Parallel Line Generation
Conference on Electronics, Telecommunication, Control and Computers CNETAC'86
Bucharest, Romania, December 4-6, 1986
- O₈ F. Moraru, C. Ispas, S. Constantin, A. Niculescu, and V. Beiu: Automat Conical Ball Bearing Sorting System
National Conference on Automatic Measurement Systems Using Computer Techniques
Bucharest, Romania, May 22-24, 1986
- O₇ V. Beiu: Parallel Adder with Regular Structure
Conference on Electronics, Telecommunication, Control and Computers CNETAC'85
Bucharest, Romania, November 21-23, 1985
- O₆ V. Beiu: Self-Testable and Self-Repairable Units – A Must for VLSI Structures
Conference on Electronics, Telecommunication, Control and Computers CNETAC'84
Bucharest, Romania, November 22-24, 1984
- O₅ V. Beiu: High Reliability Memory Organization
Conference on Electronics, Telecommunication, Control and Computers CNETAC'83
Bucharest, Romania, November 17-18, 1983
- O₄ V. Beiu: Using Microprocessors in Audio Systems
Conference on Electronics, Telecommunication, Control and Computers CNETAC'82
Bucharest, Romania, November 17-19, 1982
- O₂ V. Beiu: Method for Storing Digital Information on a Video Recorder
Conference on Electronics, Telecommunication, Control and Computers CNETAC'81
Bucharest, Romania, November, 1981

11. BDI TECHNICAL REPORTS

Remark: 25 have appeared only as technical reports, while 42 have also been published (conferences/journals)
<https://www.lanl.gov/library/find/reports/index.php>

- TR₆₇ V. Beiu: WTEC-NANO2 (21 pages)
International Study of the Long-term Impacts and Future Opportunities for
Nanoscale Science and Engineering, September 2010
- TR₆₆ V. Beiu, H.E. Makaruk, D. Morgan, and L. Popa-Simil
ARGOS Advanced RTR (Real Time Radiography) Graphical Object Selection
Los Alamos Unrestricted Report LA-UR-03-2477, April 2003
- TR₆₅ V. Beiu, H.E. Makaruk, D. Morgan, and L. Popa-Simil: ARGOS – The Problem
Los Alamos Unrestricted Report LA-UR-03-2474, April 2003
- TR₆₄ V. Beiu: On Automatic Synthesis of Analog/Digital Circuits

- Los Alamos Unrestricted Report LA-UR-98-3463, 1998
- TR₆₃ V. Beiu: Larger Bases and Mixed Analog/Digital Neural Networks
Los Alamos Unrestricted Report LA-UR-98-3462, 1998
- TR₆₂ V. Beiu, J. Frigo, and K.R. Moore: On the Reliability of Nervous Nets
Los Alamos Unrestricted Report LA-UR-98-3461, 1998
- TR₆₁ V. Beiu: Neural Inspired Parallel Computations Require Analog Processors
Los Alamos Unrestricted Report LA-UR-98-3325, 1998
- TR₆₀ V. Beiu, and S. Draghici: Designing Constructive Neural Learning Algorithms Based on Information Entropy Bounds
Los Alamos Unrestricted Report LA-UR-98-3168, 1998
- TR₅₉ V. Beiu: On Kolmogorov's Superposition and Boolean Functions
Los Alamos Unrestricted Report LA-UR-98-2883, 1998
- TR₅₈ V. Beiu: 2D Neural Hardware vs 3D Biological Ones
Los Alamos Unrestricted Report LA-UR-98-2504, 1998
- TR₅₇ V. Beiu, S. Draghici, and T. De Pauw: A Constructive Approach to Calculating Lower Entropy Bounds
Los Alamos Unrestricted Report LA-UR-98-2333, 1998
- TR₅₆ V. Beiu: Implementing Size-Optimal Discrete Neural Networks Requires Analog Circuitry
Los Alamos Unrestricted Report LA-UR-98-1702, 1998
- TR₅₅ V. Beiu, and K.R. Moore: On Analog Implementation of Discrete Neural Networks
Los Alamos Unrestricted Report LA-UR-98-1609, 1998
- TR₅₄ V. Beiu: How to Build VLSI-Efficient Neural Chips
Los Alamos Unrestricted Report LA-UR-97-4460, 1997
- TR₅₃ V. Beiu: Implementing Size-Optimal Discrete Neural Networks Requires Analog Circuitry
Los Alamos Unrestricted Report LA-UR-97-4432, 1997
- TR₅₂ V. Beiu, and H.E. Makaruk: On Deeper Nets for Classification Problems
Los Alamos Unrestricted Report LA-UR-97-4413, 1997
- TR₅₁ V. Beiu, and H.E. Makaruk: Deeper and Sparser Nets Are Optimal
Los Alamos Unrestricted Report LA-UR-97-4359, 1997
- TR₅₀ V. Beiu, S. Draghici, and H.E. Makaruk: On Limited Fan-In Optimal Neural Networks
Los Alamos Unrestricted Report LA-UR-97-4314, 1997
- TR₄₉ V. Beiu, and H.E. Makaruk: Constructive Entropy Bounds Based on n -Dimensional Complexes
Los Alamos Unrestricted Report LA-UR-97-4251, 1997
- TR₄₈ V. Beiu, and H.E. Makaruk: Small Fan-In Is Beautiful
Los Alamos Unrestricted Report LA-UR-97-3493, 1997
- TR₄₇ V. Beiu: On the Circuit and VLSI Complexity of Threshold Gate COMPARISON
Los Alamos Unrestricted Report LA-UR-97-3353, 1997
- TR₄₆ V. Beiu, and S. Draghici: On Sparsely Connected Optimal Neural Networks
Los Alamos Unrestricted Report LA-UR-97-2970, 1997
- TR₄₅ V. Beiu, and H.E. Makaruk
Computing Volumes of n -Dimensional Complexes
Los Alamos Unrestricted Report LA-UR-97-2873, 1997
- TR₄₄ V. Beiu: Entropy, Constructive Neural Learning, and VLSI Efficiency
Los Alamos Unrestricted Report LA-UR-97-2843, 1997
- TR₄₃ V. Beiu: The Next Generation of Neural Networks Chips
Los Alamos Unrestricted Report LA-UR-97-1917, 1997

- TR₄₂ V. Beiu: When Reduced Connectivity Neural Networks Are Complexity Optimal?
Los Alamos Unrestricted Report LA-UR-97-1916, 1997
- TR₄₁ V. Beiu: Digital Integrated Circuit Implementations (of Neural Networks)
Los Alamos Unrestricted Report LA-UR-97-1900, 1997
- TR₄₀ V. Beiu: Enhanced Lower Entropy Bounds with Application to Constructive Learning
Los Alamos Unrestricted Report LA-UR-97-1877, 1997
- TR₃₉ S. Draghici, V. Beiu, and I.K. Sethi: A VLSI Optimal Constructive Algorithm for Classification Problems
Los Alamos Unrestricted Report LA-UR-97-1609, 1997
- TR₃₈ V. Beiu, and S. Draghici: On Sparsely Connected Optimal Neural Networks
Los Alamos Unrestricted Report LA-UR-97-1567, 1997
- TR₃₇ V. Beiu: When Constants Are Important
Los Alamos Unrestricted Report LA-UR-97-1262, 1997
- TR₃₆ V. Beiu, S. Draghici, and T. De Pauw: A Constructive Approach to Calculating Lower Entropy Bounds
Los Alamos Unrestricted Report LA-UR-97-884, 1997
- TR₃₅ V. Beiu: Optimization of Circuits Using a Constructive Neural Network Learning Algorithm
Los Alamos Unrestricted Report LA-UR-97-851, 1997
- TR₃₄ V. Beiu: Enhanced Lower Entropy Bounds with Application to Constructive Learning
Los Alamos Unrestricted Report LA-UR-97-516, 1997
- TR₃₃ V. Beiu: Reduced Complexity Constructive Learning Algorithm
Los Alamos Unrestricted Report LA-UR-97-515, 1997
- TR₃₂ S. Draghici, and V. Beiu: Entropy Based Comparison of Neural Networks for Classification
Los Alamos Unrestricted Report LA-UR-97-483, 1997
- TR₃₁ V. Beiu, and S. Draghici: Limited Weights Neural Networks: Very Tight Entropy Based Bounds
Los Alamos Unrestricted Report LA-UR-97-294, 1997
- TR₃₀ V. Beiu: When Constants Are Important
Los Alamos Unrestricted Report LA-UR-97-226, 1997
- TR₂₉ V. Beiu: Constant Fan-In Discrete Neural Networks Are VLSI-Optimal
Los Alamos Unrestricted Report LA-UR-97-61, 1997
- TR₂₈ V. Beiu, and T. De Pauw: Tight Bounds on the Size of Neural Networks for Classification Problems
Los Alamos Unrestricted Report LA-UR-97-60, 1997
- TR₂₇ V. Beiu: Optimization of Circuits Using a Constructive Neural Network Learning Algorithm
Los Alamos Unrestricted Report LA-UR-97-59, 1997
- TR₂₆ V. Beiu: On the Circuit and VLSI Complexity of Threshold Gate COMPARISON
Los Alamos Unrestricted Report LA-UR-96-3591, 1996
- TR₂₅ V. Beiu: New VLSI Complexity Results for Threshold Gate COMPARISON
Los Alamos Unrestricted Report LA-UR-96-3576, 1996
- TR₂₄ J.C. Lemm, V. Beiu, and J.G. Taylor: Density Estimation as a Preprocessing Step for Constructive Algorithms
Munster University Technical Report MS-TPI-95-10, 1995
- TR₂₃ V. Beiu, D.C. Ioan, M. Dumbrava, and O. Robciuc
Physical Fields Determination Using Continuous Boltzmann Machines
Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, December 1991
- TR₂₂ V. Beiu: Motion Detection with Neural Networks
Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, September 1991
- TR₂₁ V. Beiu: Neural Network Solutions for Motion Detection

- Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, March 1991
- TR₂₀ V. Beiu: Neural Network Priority Queue
 Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, October 1990
- TR₁₉ A. Florea, V. Beiu, and S. Georgescu: Expert System Development with a Neural Network Simulator
 Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, December 1989
- TR₁₈ V. Beiu: From Systolic Arrays to Neural Networks
 Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, November 1989
- TR₁₇ M. Constantinescu, and V. Beiu: Theoretical Aspects of Parallel Algorithms for Histogram Modification
 Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, October 1989
- TR₁₆ V. Beiu, and A. Florea: Basic Structure of a Program Used to Simulate Processor Networks
 Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, December 1988
- TR₁₅ A. Florea, and V. Beiu: Expert Decisions Using Neural Models
 Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, December 1988
- TR₁₄ V. Beiu: Hierarchical Memory Enhanced with List Processing Facilities
 Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, October 1988
- TR₁₃ V. Beiu: Parallel Line-Drawing Algorithms
 Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, October 1988
- TR₁₂ V. Ivanov, and V. Beiu: Heuristic Simulation of Circuits Using PROLOG
 Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, February 1988
- TR₁₁ V. Beiu, M. Ionescu, E. Paşol, and L. Zuzu: VLSI Implementation of a Statistical Multiplexer
 Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, September 1987
- TR₁₀ V. Beiu, M. Ionescu, E. Paşol, and L. Zuzu: Adaptive Multiplexing Algorithm and Its Possible VLSI Implementation
 Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, April 1987
- TR₉ V. Beiu: Smart Image Memory for Parallel Line Generation
 Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, December 1986
- TR₈ F. Moraru, C. Ispas, S. Constantin, A. Niculescu, and V. Beiu: Automat Conical Ball Bearing Sorting System
 Technical Report, Department of Mechanics, University "Politehnica" of Bucharest, Romania, June 1986
- TR₇ V. Beiu: Parallel Adder with Regular Structure
 Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, December 1985
- TR₆ V. Beiu: Self-Testable and Self-Repairable Units: A Must for VLSI Structures
 Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, December 1984
- TR₅ V. Beiu: Highly Reliable Memory Organization
 Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, December 1983
- TR₄ V. Beiu: Memory Structure with Simultaneous Read and Write Capabilities
 Technical Report, Military Academy of Sciences, Bucharest, Romania, November 1982
- TR₃ V. Beiu: Using Microprocessors in Audio Systems
 Technical Report, Research Institute for Computer Technique, Bucharest, Romania, December 1982
- TR₂ V. Beiu: Method for Recording Digital Information on a Video Recorder
 Technical Report, Research Institute for Computer Technique, Bucharest, Romania, December 1981
- TR₁ V. Beiu: Reliability Enhanced Memory with Gracefully Degrading Performances
 Technical Report, Research Institute for Computer Technique, Bucharest, Romania, July 1981

11. PATENTS 5 ARE INDEXED IN ISI WoS AS ARTICLES, HENCE THEY ARE ALSO REPORTED UNDER #1

P₁₁ V. Beiu: Low-Power Differential Conductance-Based Logic Gate and Method of Operation Thereof
 US 6,580,296, June 17, 2003 1-18
<https://patents.google.com/patent/US6580296/> DIIDW:2003656312

P₁₀ V. Beiu: Microprocessor and a Digital Signal Processor Including Adder and Multiplier Circuits
 Employing Logic Gates Having Discrete and Weighted Inputs
 US 6,516,331, February 4, 2003 1-14
<https://patents.google.com/patent/US6516331/> DIIDW:2000349800

P₉ V. Beiu: Adder Circuits Employing Logic Gates Having Discrete Weighted Inputs and a
 Method of Operation Therewith
 US 6,502,120, December 31, 2002 1-13
<https://patents.google.com/patent/US6502120/>

P₈ V. Beiu: Adder Having Reduced Number of Internal Layers and Method of Operation Thereof
 US 6,438,572, August 20, 2002 [Also as WO/2001/023992 and AU40251/01] 1-11
<https://patents.google.com/patent/US6438572/> DIIDW:2001316145

P₇ V. Beiu: Noise Tolerant Conductance-Based Logic Gate and Methods of Operation and
 Manufacturing Thereof
 US 6,430,585, August 6, 2002 [Also as WO/2001/024367 and AU76009/00] 1-16
<https://patents.google.com/patent/US6430585/> DIIDW:2001281699

P₆ V. Beiu: Adder Having Reduced Number of Internal Layers and Method of Operation Thereof
 TW 493139, July 1, 2002 1-15
https://twpat1.tipo.gov.tw/tipotwoc/tipotwekm?!FR_493139

P₅ V. Beiu: Noise Tolerant Conductance-Based Logic Gate and Methods of Operation and
 Manufacturing Thereof
 TW 483249, April 11, 2002 1-13
https://twpat1.tipo.gov.tw/tipotwoc/tipotwekm?!FR_483249

P₄ V. Beiu: Adder and Multiplier Circuits Employing Logic Gates Having Discrete, Weighted Inputs
 and Methods of Performing Combinatorial Operations Therewith
 TW 481774, April 1, 2002 1-14
https://twpat1.tipo.gov.tw/tipotwoc/tipotwekm?!FR_481774

P₃ V. Beiu: Logic Gate Having Reduced Power Dissipation and Method of Operation Thereof
 US 6,259,275, July 10, 2001 1-19
<https://patents.google.com/patent/US6259275/> DIIDW:2001595137

P₂ V. Beiu: Adder and Multiplier Circuits Employing Logic Gates Having Discrete, Weighted Inputs
 and Methods of Performing Combinatorial Operations Therewith
 US 6,205,458, March 20, 2001 [Also as WO/2000/017802 and AU58155/99] 1-14
<https://patents.google.com/patent/US6205458/>

P₁ V. Beiu: LSI Unit for Mutual Exclusion
 RO 84763, April 26, 1984 1-12

12. RESEARCH GRANTS

2020	• Short term travel grants (invited): ICCCC'20 (US\$ 500)		0.5K\$
2019	• Short term travel grants (invited): ECC'19 (US\$ 300)		0.3K\$
2018	• Short term travel grants (invited): ICCCC'18 (US\$ 800), SOFA'18 (US\$ 600)		1.4K\$
2016 – 2021	• Novel Bio-inspired Cellular Nano-architectures	PI	9.3MRON
BioCELL-NANOART	With V.-F. Duma (UAV), F.-D. Munteanu (UAV), C. Stoica (UAV), P. Gaspar (UAV), V.E. Balas (UAV), M. Balas (UAV), A. Cavaco-Paulo (U Minho), L. Daus (UTC Bucharest)	POC-A1-A1.1.3-E nr. 30/2016	
2016	– Short term travel grants (invited): ICCCC'16 (US\$ 500), SOFA'16 (US\$ 500) IEEE-NANO'16 (US\$ 1,000)		2K\$
2014 – 2016	– ATIC-SRC Center of Excellence in Energy Efficient Electronic Systems (ACE ⁴ S) Task: Ultra-low Power Digital Sub-threshold FinFET Amplifiers Originally with G. Fettweis (TU Dresden) and M. Alioto (Natl. U Singapore)	Co-PI	35MAED
ULP-DigiFinA	https://www.src.org/newsroom/press-release/2013/452/	SRC	GRC ACE ⁴ S
2013 – 2016	– Strengthening Research Collaborations in High-impact and Emerging Technologies between GCC and EU	Co-PI	1.23M€
SECRET	With <i>B. Aziz M. Rahman</i> PI (City U London), G. Cuniberti (TU Dresden), V. Hessel (TU Eindhoven), O. Benitez (U Deusto), P. Candeloro (U Magna Graecia), C. Themistos (Frederick U), H. Bourdoucen (Sultan Qaboos U), F. Bou-Rabee (Kuwait U), S.A. Al-Mansoori (U Bahrain), F. Kharbash (UAEU)	EU EM 545790-EM-1-2013-1-UK-ERA MUNDUS-EMA22	
2012 – 2015	– Synaptic Molecular Networks for Bio-inspired Information Processing	Co-PI	2.81M€
SYMONE	With <i>G. Wendin</i> PI (Chalmers U), D. Vuillaume (CNRS-IEMN), J. Roncali (CNRS-MOLTECH), M. Calame (Basel U), S. Yitzchaik (HUJI), C. Gamrat (CEA), and G. Cuniberti (TU Dresden)	EU FP7-ICT-318597	
2012 – 2014	– Unconventional Sizing for Enabling Low Power Digital Design	PI	200K\$
Use-LP	With M. Alioto (U Siena/Natl. U Singapore), A. Beg (UAEU), W. Ibrahim (UAEU), and F. Kharbash (UAEU)	SRC	2012-TJ-2332
2011 –	• Ultra Low-Power Application-specific Non-Boolean Architectures [Intel Co]	Co-PI	1M\$
ULP-NBA	With <i>Intel</i> PI, D. Hammerstrom (Portland State U), W. Porod (U Notre Dame), S.P. Levitan (U Pittsburgh), T. Shibata (U Tokyo), T. Roska (Hungarian Acad. Sci.), M. Pufall (NIST), D. Weistein (MIT), and M.R. Stan (U Virginia)	URO	2011-05-24G
2011 – 2015	– Ultra Low Power NEMS-CMOS	PI	300K\$
ULP-NEMS-CMOS	With T.-J.K. Liu (UC Berkeley), W. Ibrahim (UAEU), and A. Beg (UAEU)	SRC	2011-HJ-2184
2011 – 2013	– Brain-inspired Interconnects for Nanoelectronics (BiIN)	PI	586KAED
	With W. Ibrahim (UAEU) [UAE Natl. Res. Found.]	NRF	1108-00451
2011 – 2013	– Algorithms & EDA for Accurate Nano-Circuits Reliability Calculations (CREDA ²)	Co-PI	506KAED
	With <i>W. Ibrahim</i> PI (UAEU) [UAE Natl. Res. Found.]	NRF	1108-00329
2013	– Short term travel grants (invited): TUDresden (US\$ 7,000)		7K\$
2012	– Short term travel grants (invited): EDCC'12 (US\$ 1,000)		1K\$
2011	– Short term travel grants (invited): IEEE-NANO'11 (US\$ 500), EU Brussels (US\$ 8,000), EU Paris (US\$ 5,000), NSF (US\$ 5,000), ATIC-SRC (US\$ 10,000)		28.5K\$
2011 – 2012	– Brain-inspired Hybrid Topologies for Nano-architectures [SRC 2011-RJ-2150G]	PI	40K\$
2010	– Short term travel grants (invited): IDT'10 (US\$ 500), IJCNN'10 (US\$ 1,500), INC6 (US\$ 1,000), MEES'10 (US\$ 3,000)		6K\$
2009 – 2011	– Brain-inspired Interconnects for Nanoelectronics [British Council PMI2 RCGS271]	PI	39KUK€
2009 [on hold]	– Emirates Center for Nanoscience & Nanoengineering [UAE Natl. Res. Found.]	Co-PI	50MAED
	http://www.thenational.ae/news/uae-news/education/grant-aids-research-centres		
2009	– Short term travel grants (invited): EU (US\$ 7,000), U Oslo (US\$ 5,000), IEEE-		20.5K\$

	NANO'09 (US\$ 1,000), ESSCIRC'09 (US\$ 1,500), NanoNet'09 (US\$ 1,000), WDSN'09 (US\$ 5,000)		
2008	– Short term travel grants (invited): NSF (US\$ 5,000), LANL (US\$ 2,000), SAMOS VIII (US\$ 5,000), Tohoku U (US\$ 10,000), U Paris-Sud (US\$ 3,000), U Oslo (US\$ 5,000)		33K\$
2007	– Short term travel grants (invited): NSF (US\$ 5,000), EU (US\$ 8,000), HP Labs (US\$ 6,000), FENA/UCLA (US\$ 1,000), ULSIWS'07 (US\$ 400), ISMVL'07 (US\$ 1,000), SHARCS'07 (US\$ 2,000), DTIS'07 (US\$ 3,000), DCIS'07 (US\$ 3,000), IECON'07 (US\$ 3,000), Tohoku U (US\$ 5,000), MWSCAS'07 (US\$ 1,000), IEEE-NANO'07 (US\$ 1,000), ICSPC'07 (US\$ 500), ICTRF'07 (US\$ 500), IDT'07 (US\$ 500), IWANN'07 (US\$ 5,000), NanoMaterials'07 (US\$ 500), Univ. Oslo (US\$ 5,000)		51.4K\$
2006 – 2011	– Center for Excellence in Intelligent Systems [InvestNI, IDF and U Ulster] Co-PI Center for Neural Inspired Nano Architectures (~1.8MUK£, 2007–2010)		20.4MUK£
2007	– Mapping the proxel method to reliability analysis of nanoarchitectures [UAEU]	Co-PI	8KAED
2006	– Short term travel grants (invited): NSF (US\$ 5,000), WNEC'06 (US\$ 2,500), IDT'06 (US\$ 500), AICCSA'06 (US\$ 500)		8.5K\$
2006	– Investigation of the reliability of single electron technology gates & circuits [UAEU]	Co-PI	8KAED
2005	– Short term travel grants (invited): ICM'05 (US\$ 3,000), U Ulster (US\$ 9,000), SNB'05 (US\$ 3,000), IIT'05 (US\$ 1,000)		16K\$
2005 – 2006	– Defect-tolerant high-performance low-power computing with hybrid CMOS molecular circuits [Advanced Research & Development Agency, ARDA]	Co-PI	100K\$
2004	– Short term travel grants (invited): ASAP'04 (US\$ 500), NGCM'04 (US\$ 1,000), IJCNN'04 (US\$ 500), Heinz Nixdorf Inst. (US\$ 1,500)		3.5K\$
2003	– Short term travel grants (invited): MWSCAS'03 (US\$ 500), ICNNSP'03 (US\$ 500), NIPS'03 (US\$ 500), U Paderborn (US\$ 1,500), IJCNN'03 (US\$ 500), IWANN'03 (US\$ 500), NCI'03 (US\$ 500), Heinz Nixdorf Inst. (US\$ 2,000)		6.5K\$
2002 – 2004	– Direct Digital Frequency Synthesizers (DDFSs) for reconfigurable communication systems. DDFSs have been investigated and implemented in silicon-on-insulator (SOI) and CMOS for space applications [Air Force Research Lab/CDADIC]	Co-PI	250K\$
2002	– Short term travel grant (invited): LANL, Los Alamos (US\$ 5,000)		5K\$
2001	– Short term travel grant (invited): Berkeley Wireless Research Center (US\$ 4,000)		4K\$
2000 – 2003	– Conducting research on ultra-fast low-power floating point units (FPUs), with applications to graphic accelerators and gaming workstations [Rose Research]	PI	500K\$
2000 – 2003	– Evaluating/examining solutions for ultra-fast low-power encryption/decryption allowing for wire-speed (i.e., on-the-fly) crypto-processors [Rose Research]	PI	500K\$
1999 – 2005	– Pioneered <i>FastLogic</i> , an enabling VLSI technology based on novel ultra-fast logic gates, and a systematic design methodology for using them. Low-power was achieved by means of a novel self-timed power-down mechanisms, as well as differential (charge recycling) circuits. Several versions of <i>FastLogic</i> gates have been designed, simulated, tested, and patented (during 1999-2001). Ultra-low power sub-threshold versions have also been designed using an original cross-coupled adaptive body biasing scheme for boosting reliability. [Rose Research]	PI	3M\$
1999 – 2002	– Exploring alternatives and improving on ultra-fast low-power multiplication and multiply-accumulate with application to digital signal processing [Rose Research]	PI	1M\$
1999	– Short term travel grant (invited): AMS-SMM'99 (US\$ 500)		0.5K\$
1998 – 1999	– Researched, analyzed and enhanced ultra-fast VLSI adders. The theoretical results obtained have been verified and patented. [Rose Research]	PI	500K\$
1998	– Short term travel grants (invited): NC'98 (US\$ 500), CNRS-Paris (US\$ 1,000), PARELEC'98 (US\$ 500), EIS'98 (US\$ 1,000)		3K\$
1997	– Short term travel grants (invited): SBRN'97 (US\$ 5,000), IDIAP, Switzerland (US\$ 2,000), Heinz Nixdorf Inst. (US\$ 1,500), U Paris XII (US\$ 1,000), Royal		12.1K\$

	Holloway U (US\$ 1,000), Oxford U (US\$ 1,000), NEuroTop'97 (US\$ 600)		
1996 – 1998	– Field Programmable Neural Arrays (FPNAs) as a component of the Deployable Adaptive Processing Systems (DAPS) carried out at Los Alamos National Laboratory (LANL). This was a multi-faceted R&D program, developing algorithms and prototyping systems for real-time remote and autonomous processing of data gathered on land, in the air, or in space. Specified and designed neural-inspired adaptive algorithms and their mapping onto FPGAs.	PI	180K\$
1996	– Short term travel grants (invited): ANITA'96 (US\$ 1,500), SBRN'96 (US\$ 2,500), AT'96 (US\$ 500)		4.5K\$
1995	– Short term travel grants (invited): ADT'95 (US\$ 500)		0.5K\$
1994 – 1996	– Programmable Neural Arrays, Design & VLSI Implementation of Neural Networks Using Threshold Gates [EU CHBICT941741]	PI	440K\$
1992 – 1994	– VLSI-efficient threshold logic gates (Concerted Research Action of the Flemish Community)		21K\$
1994	– Short term travel grants (invited): ConTI'94 (US\$ 300), EMCSR'94 (US\$ 300), RRCS'94 (US\$ 500)		1.1K\$
1993	– Short term travel grants (invited): ROSYCS'93 (US\$ 300), ESSAN'93 (US\$ 600)		0.9K\$
1992	– Short term travel grant (invited): EPFL (US\$ 500)		0.5K\$
1991	– Short term travel grants (invited): ICIAM'91 (US\$ 1,500), ICANN'91 (US\$ 1,500)		3K\$
1991	– Expert of DEANNA (Data-base for European Artificial Neural Network Activity), an ESPRIT exploratory action led by JENNI (Joint European Neural Network Initiative)		
1990 – 1991	– Negotiated, won, managed, and coordinated SPRING Software Consult contracts		
	» Dedicated En/Decryption and GUI [Ministry of National Defense]	PI	20K\$
	» CAD Training (lectures) [AVERSA SA]	PI	5K\$
	» Software Package for Microbusiness [Chemistry Research Institute]	Co-PI	10K\$
	» Data Acquisition CAD Package [Chemistry Research Institute]	PI	10K\$
	» PC Training (lectures) [Ministry of National Defense]	PI	5K\$
1990	– Short term travel grant (invited): PARCELLA'90 (US\$ 300)		0.3K\$
1988	– Dedicated watch-dog system: Feasibility study & reliability analysis [Electrical Networks Institute]	PI	50K\$
1987 – 1988	– Studied and analyzed Prolog as a research tool for circuit simulations [UPB]	Co-PI	
1987	– Short term travel grant (invited): ComEuro'87 (US\$ 400)		0.4K\$
1987	– Dedicated Database Package [National Information & Documentation Institute]	PI	50K\$
1987	– Hierarchical Self-testable and Self-repairable Content Addressable Memory [UPB]	PI	50K\$
	– High Speed Antialiasing Cascadable Circuit [UPB]	PI	50K\$
1984 – 1987	– VLSI CAD Package (PC version) [UPB]	PI	100K\$
	– Automatic Conical Ball Bearing Sorter [Bearings Factory Alexandria, now Koyo]	PI	100K\$
1983	– Mutual exclusion circuit (patented) [Research Institute for Computer Techniques]		PI
	– Floppy disk interface [Research Institute for Computer Techniques]		
1981 – 1982	– Ultra high-speed floating point unit. New improved algorithms with innovations at the microprogramming level [Research Institute for Computer Techniques]	PI	
1981	– Ultra high-speed highly reliable central processing unit with enhancements at the microprogramming level [Research Institute for Computer Techniques]	PI	
1980	– Involved in the final testing stages of the CE-100 computer (PDP equivalent)	Co-PI	
1979 – 1980	– High speed graphic workstation: 1024×1024 with 16 intensities [UPB] 20 MHz HP vectorial display and original CPU design (tested at 60 MHz) » Three Best Paper Awards at the Students' Scientific Research Conference » Best MSc Thesis Award for "innovations in workstation design"		5K\$
1977 – 1980	– National Merit Scholarship [Ministry of Science & Education]		10K\$