VALERIU BEIU — PUBLICATIONS

OVERVIEW	PUBLISHED	ACCEPTED
BOOKS	2	3
CHAPTERS	8 (7 INVITED)	5
PATENTS	20	
JOURNALS	43 (2 INVITED)	3 (1 INVITED)
CONFERENCES	225 (28 INVITED)	
TOTAL	309 (38 INVITED, 8 BEST PAPER AWARDS)	
OTHER CONFERENCES	53 (7 INVITED, 1 BEST PAPER AWARD)	
TECHNICAL REPORTS	73	

BOOKS 2

– V. Beiu and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures
Book in progress (contract signed with World Scientific)

– V. Beiu: VLSI Complexity of Discrete Neural Networks
Book in progress (contract signed with Taylor & Francis)

– V. Beiu, R. Andonie, and R. Dogaru: Fundamental Problems of Neural Networks
Book in progress (contract signed with Technical Printing House)

B_2 V. Beiu and S. Harous (Eds.): Innovations
IEEE Press, November 2014 (ISBN 9781479972128) 1–132
https://doi.org/10.1109/INNOVATIONS.2014.6985768

B_1 A. Schmid, S. Goel, W. Wang, V. Beiu, and S. Carrara (Eds.): Nano-Net
Springer, LNICS, October 2009 (ISBN 9783642024276) 1–286
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··· V. Beiu: Neural Networks Using Threshold Gates
A Complexity Analysis of Their Area- and Time-Efficient VLSI Implementations
PhD dissertation (*summa cum laude*), Katholieke Universiteit Leuven, Leuven, Belgium
U.D.C. 621.3.04977: 681.3*C13 (x-27-151779-3), May 1994 1–222

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– V. Beiu and W. Ibrahim: On Enabling Redundant Designs for Nano Computations
In V. Beiu and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures

– V. Beiu, J.M. Quintana, and M.J. Avedillo
Threshold Logic Design and Implementations: From the Early Days into the Nanoera
In V. Beiu and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures

– M.H. Sulieman and V. Beiu
From Single Electron Technology (SET) Full Adders to Optimal Practical SET Adders
In V. Beiu and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures

– V. Beiu and U. Rückert: Roadmap for Nano Architectures
In V. Beiu and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures

– J. Nyathi, and V. Beiu: Advanced Techniques for Reducing Power Consumption
In V. Beiu and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures

Ch_8 V. Beiu, L. Zhang, A. Beg, W. Ibrahim, and M. Tache: Axon-Inspired Communication Systems *Invited*$_7$
Chapter 15 in J.E. Morris and K. Iniewski (Eds.): Nanoelectronic Device Applications Handbook, CRC/Taylor & Francis (UK/USA), 2013 (ISBN 9781466565234) 193–208

Ch_7 A. Beg, M.H. Sulieman, V. Beiu, and W. Ibrahim: Low-Power Reliable Nano Adders ***Invited$_6$***
Chapter 6 in J.E. Morris and K. Iniewski (Eds.): Nanoelectronic Device Applications Handbook, CRC/Taylor & Francis (UK/USA), 2013 (ISBN 9781466565234) 67–75

Ch_6 V. Beiu, W. Ibrahim, and S. Lazarova-Molnar
On Device-level Majority von Neumann Multiplexing ***Invited$_5$***
Chapter 72 in J.R. Rabuñal et al. (Eds.): Encyclopedia of Artificial Intelligence
IGI Global, USA (Hershey, PA) and UK (London), 2009 (ISBN 9781599048499) 471–479
https://doi.org/10.4018/978-1-59904-849-9.ch072

Ch_5 V. Beiu and W. Ibrahim: On Computing Nano-Architectures Using Unreliable Nano-Devices ***Invited$_4$***
Chapter 12 in S.E. Lyshevski (Ed.): Nano- and Molecular-Electronics Handbook
Taylor & Francis (UK/USA), May 2007 (ISBN 9780849385285) 1–49

Ch_4 V. Beiu: Entropy, Constructive Neural Learning, and VLSI Efficiency ***Invited$_3$***
In R. Andonie, and D. Grosu (Eds.): Neural Priorities in Data Transmission and EDA
Tempus SJEP 8180-94, "Transilvania" Univ. of Braşov, Braşov, Romania, 1998 38–74
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Ch_2 V. Beiu: Digital Integrated Circuit Implementations (of Neural Networks) ***Invited$_2$***
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Ch_1 V. Beiu: Optimal VLSI Implementations of Neural Networks ***Invited$_1$***
Chapter 18 in J.G. Taylor (Ed.): Neural Networks and Their Applications
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– V. Beiu: Procedure Enabling Statistical Meaningful Evaluation of Any Physical Feature or Figure-of-Merit of a Digital or Analog Circuit
UAEU Intellectual Property Disclosure, Jul. 16, 2014 & Feb. 11, 2015 (Rouse Ref. U0018-00167)

P_{20} V. Beiu: Low-Power Differential Conductance-Based Logic Gate and Method of Operation Thereof
(Washington, DC, USA, June 17, 2003) 1–18
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TW 493139 https://www.tipo.gov.tw/en/mp-2.html (do a search)
US39682800 https://patentscope.wipo.int/search/en/detail.jsf?docId=US39682800
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$P_{9\text{-}12}$ V. Beiu: Noise Tolerant Conductance-Based Logic Gate and Methods of Operation and Manufacturing Thereof (Washington, DC, USA, August 6, 2002) 1–16
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⋯ V. Beiu et al.: The Curse of Constant Failure Rates, Inputs and Averaging – A Comprehensive Review
⋯ V. Beiu et al.: Brain-inspired Computing Revisited – Why Energy Consumption Is So Elusive
⋯ V. Beiu, R.-M. Beiu, and V. Dragoi: The Trustworthy Wings of the Mysterious Butterflies
⋯ M. Jianu, M. Jianu, L. Daus, and V. Beiu:
Computing the Reliability of Hammock Networks in Quadratic Time with Respect to Length
⋯ V. Beiu and M. Tache: Revisiting Schmitt Trigger Tolerance to Variations
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